TI's new C2000™ real-time controller series: TMS320F28002x

2020 Q2

Agenda

- C2000™ + TMS320F28002x introduction

- C2000™ Generation 3 Enhancements

- Available C2000™ F28002x-based solutions + how to get started

- C2000™ peripheral deep dive
  - FSI: What can you do with a low-latency 200Mbps serial interface?
  - CLB: Defy conventional logic with customizable on-chip peripherals

- C2000™ Digital Control Library Overview
  - Non-linear PID (new in F28002x)

TEXAS INSTRUMENTS

F28002x real-time controllers:
Real-time control meets system cost optimization and performance scalability

Single-axis servo

variable frequency drives

Appliances

Server power

Telecom power

TEXAS INSTRUMENTS

The latest in extensive real-time control portfolio

- The F28002x series builds on **the third generation** improvements introduced in the F2838x, F2837x and F28004x series.
- The F28002x series allows to scale from high-end to mid-end to **low-end** while maintains differentiation and performance.
- The C2000 portfolio provides **pin-to-pin** and code compatibility, alleviating effort to scale products performance.
- It's **easy to migrate** and build a range of products on similar technology, enabling a sustainable platform solution.
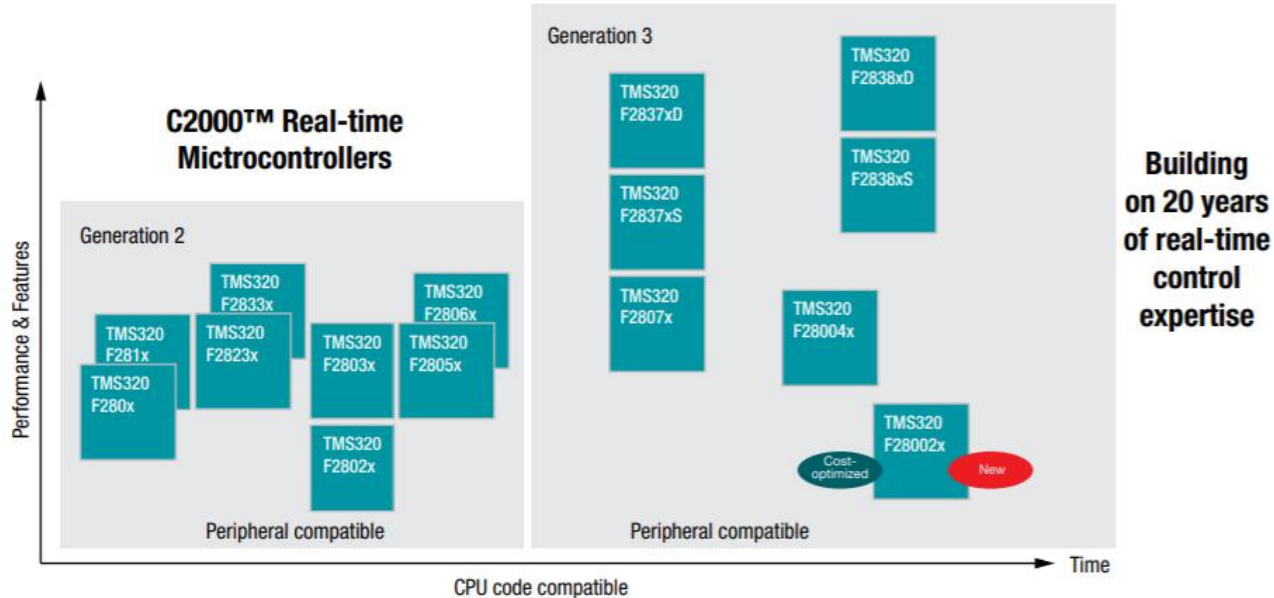
C2000™ F28002x

FCS: Now   APL: April'20   RTM: October'20

Differentiation

Optimized for Low-Cost, High-Performance Power Control Applications

Streamlined performance
- 100MHz / 128 kB flash / 28 kB SRAM
- 100 MIPS DSP Processing Power
- Floating Point, Trigonometric Math Unit, NLPID & Division acceleration

Advanced actuation and design flexibility
- 4th gen ePWM enables implementation of the most advanced switching techniques for increased efficiency and power density
- Enhanced crossbars provide flexibility in combining inputs, outputs and internal resources for advanced control and protection mechanisms

Premium analog
- 2 12-bit 3.45MSPS ADC with post processing and threshold actions
- 4 Windowed Comparator Sub-system

Rich digital options
- CAN, QEP, Position Manager, UART, SPI, LIN, I2C, PMBus, FSI, etc.

Perfect portfolio
- Architecture compatible with F28004x, F2807x, and F2837x
- Pin-pin compatible with 64-pin F28004x
- Upgrade for popular Piccolo F2803x and F2802x

F28002x

Temperatures	125C	Q100

Sensing
- ADC1: 12-bit, 3.45 MSPS, 8ch
- ADC2: 12-bit, 3.45 MSPS, 8ch
- 4x CMPSS : 12-bit DAC 8 COMP, 8 digital filters
- Temperature Sensor
- 2x eQEP
- 3x eCAP , 1x HRCAP

C28x™ DSP core 100 MHz
- FPU, FastDIV
- TMU w/ NLPID
- 6ch DMA
- CRC & HWBIST

Actuation
- 7x ePWM Modules 14x Outputs (8x High-Res)
- Fault Trip Zones

Connectivity
- 1x UART, 2x LIN/UART
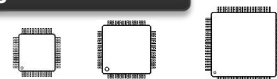- 1x I2C, 1x PMBus
- 2x SPI, 1x FSI
- 1x CAN 2.0B

Configurable Logic Block
- 2 Tiles

Memory
- 128 kB FLASH (1 bank) +ECC
- 24 kB SRAM +ECC
- ROM
- 128-bit Dual Security Zones
- Host Interface Controller (HIC)

Power & Clocking
- 2x 10 MHz OSC
- 1.2V VREG
- POR/BOR Protection

System Modules
- 3x 32-bit CPU Timers
- NMI Watchdog Timer
- 192 Interrupt PIE

Debug
- cJTAG / Real-time JTAG
- ERAD

Tools

Experimenter's Kit
Part Number: TMDSCNCD280025C
'20Q2

LaunchPad
Part Number: LAUNCHXL-F280025C
'21Q2

Software

C2000Ware™ Software Package

Application SDKs

Packages

Package	Footprint Dimensions	Temp
48-pin LQFP	9 x 9 mm	S, Q
64-pin LQFP	12 x 12 mm	S, Q
80-pin LQFP	14 x 14 mm	S, Q

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C2000™ generation 3 enhancements

F2838x, F2837x, F2807x, F28004x, **F28002x**

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F28002x comparison table

F28002x Highlights

- F28002x is a new and improved migration device for the popular F2802x/03x devices at an even lower cost

- FPU (floating point) + FastDIV functionality

- Accelerators (TMU, DMA)
  - NonLinear PID to boost efficiency for applications that demand especially fast transient response

- 2 ADCs with individual sample and hold, post processing and more flexible triggering

- NEW Host Interface Controller

- Feature rich comparator sub-system

- Variety of serial channels: FSI, PMBus, LIN, I2C, SPI, CAN, QEP, more

Comparison of F28002x series with Gen 2 and Gen 3 series

	GEN 3		GEN 2	
	F280025	F280049	F28027	F28035
Total MIPS	100	200	60	120
CPU	100	100	60	60
FPU	YES + FastDIV	YES	NO	NO
TMU	YES + NLPID	YES	NO	NO
DMA	YES	YES	NO	NO
CLA	NO	Type-2	NO	Type-1
Flash (KB)	128	256	64	128
RAM (KB)	24	100	20	20
ADC	2x12-bit	3x 12 bit	1X 12-bit	1x 12-bit
Sample & Hold	2	3	2	2
ADC Channels	16	21	16	16
ADC Post Processing	YES	YES	NO	NO
Comparators	4	7	2	3
CMPSS	CMPSS	CMPSS	NO	NO
Sigma-Delta Filter	0	4	0	0
ePWM Technology	Type-4	Type-4	Type-2	Type-2
PWM Channels	14	16	14	14
HRPWM Channels	8	16	7	7
CLB	YES	YES	NO	NO
HIC	YES	NO	NO	NO
QEP	2	2	0	1
CAN	1	2	0	1
UART	3	2	1	1
LIN	2	1	0	0
I2C	2	1	1	1
SPI	2	2	1	2
FSI	1	1	0	0
PMBus	1	1	0	0
Packages	48, 64, 80	56,64,100	38,48	56, 64, 80
1ku price	$1.52 - $3.30	$4.85 - $7.95	$2.20 - $4.08	$3.05 - $5.80

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C2000™ Generation 3 Enhancements

New process technology allows for more features: accelerators (TMU), memory, peripherals, lower power consumption.

Modules	Enhancement
ePWM	flexible load capability, DB generation, advance trip-zone functionality, more high resolution PWMs
X-BAR	flexible crossbars for premium advanced control and protection mechanisms
ADC	Improvements to sensing capability through additional ADCs, and ADC post-processing hardware
CMPSS	new Comparator Subsystem (CMPSS) with windowed comparators
FSI	latest peripherals like high-speed Fast Serial Interface (FSI) at up to 200 Mbps
CLB	new Configurable Logic Block (CLB) provides further system integration and customization
Memory	enhancements with addition of ECC, parity, dual-zone security memory and DMA

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C2000™ F28002x solutions & get started

Two phase, interleaved LLC DC-DC Converter for EV/HEV Applications

Design Status: F28002x support DPSDK, legacy F2837xD support in ControlSUITE

TIDesigns

Features

- Two-phase interleaved LLC resonant DC-DC solution showcasing type-4 PWM, ADC and CMPSS features on C2000 real-time controller
- V_{in}: 370V – 410VDC, V_{out}: 12VDC, I_{out}: 42.5A, P_{out}: 500W
- Peak efficiency: 94.5%, Efficiency > 90% (loads >10%)
- Switching frequency: 200-350 kHz (Resonant 250 kHz)
- Software based current sharing
- Configurable phase shedding, soft-start, and SR limits
- Fault protection: primary current, output voltage and current
- PMBUS library can be added

Applications

- EV 400V to 12V DC-DC
- Server power supplies
- Telecom power supplies

Tools & Resources

- **TIDM-1001**
- **Design Guide**
- **Design Files:** Schematics, BOM, Gerbers, Software, etc.
- Device Datasheets:
  – TMS320F280025C
  – UCD7138
  – UCC27524

Benefits

- Cost effective F28002x device
- Type-4 PWM enables control of multi-phase resonant converters without SW overhead and constraints
- Current balancing with no additional hardware achieves << 5% phase mismatch
- PowerSUITE GUI and SDK support enables easy evaluation and development

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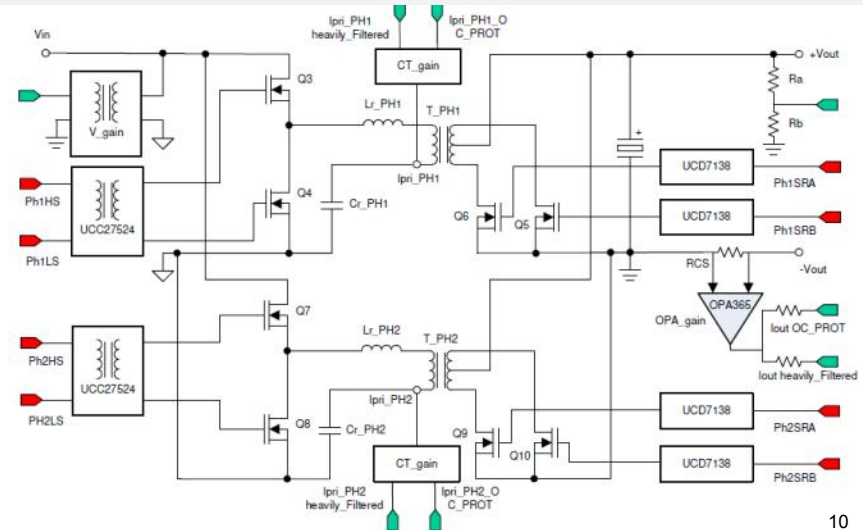
Encoder based Servo Drive

- Low-cost, single-chip high-voltage servo drive
- Fast Current Loop FOC
  - PWM latency and FOC execution time signally improve by using Floating Point Unit (FPU), Trigonometric Math Unit (TMU) and Fast Integer Division Unit (FINTDIV)
  - < 2.0us current loop (PWM update), > 96% modulation index to achieve higher speeds
- Dynamic analysis using SFRA
 - Noise is injected into the current loop and output response is measured/ analyzed

Applications

- Industrial servo drives
- Factory automation and control
- Robotics

Tools & Resources

- **MotorControl SDK**
- **Key TI Device:**
  TMS320F280025C
- **Development Board:**
  – TMDXCNCD28025C
  – TMDXIDDK379D

Benefits

- Cost effective F28002x real-time controller
- Improve current loop stability at higher speeds
- Reduce inverter power dissipation
- Easily measure performance in terms of stability and closed loop bandwidth

Sensored-FOC based F28002x

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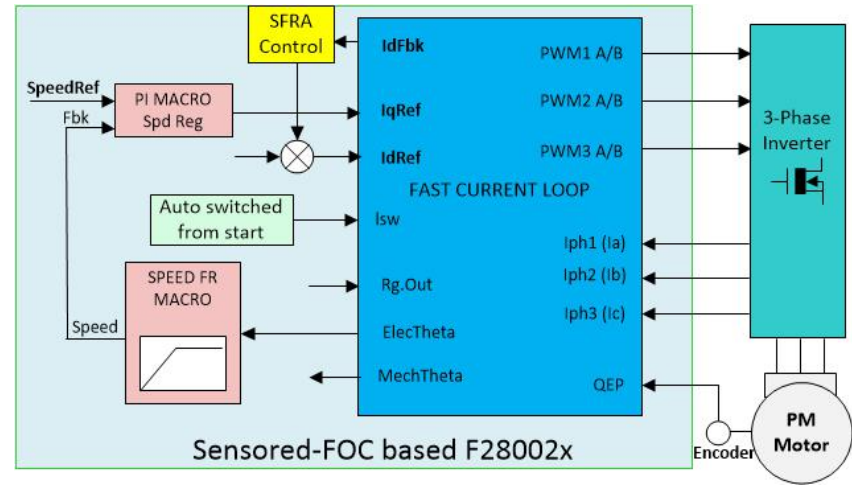
Fast Current Loop Performance
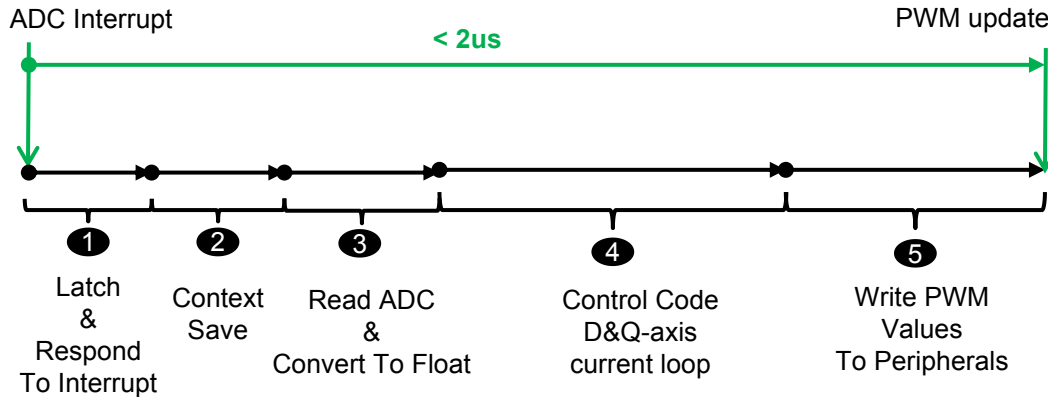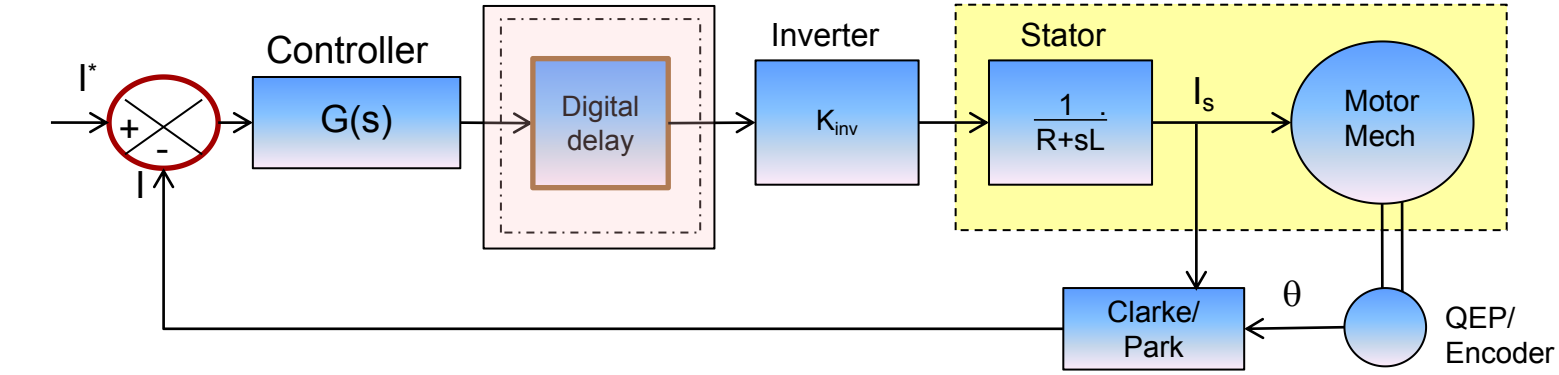
Results (10kHz PWM Frequency)
- Current loop phase margin > 60°
- > 3kHz current loop bandwidth
- > 96% modulation index
- < 2.0us current loop &PWM update
- < 7.0us FOC execution time

TEXAS INSTRUMENTS

C2000™ peripheral deep dive:
What can you do with a low-latency 200Mbps serial interface?

An introduction to Fast Serial Interface (FSI)

# Standard communication interfaces
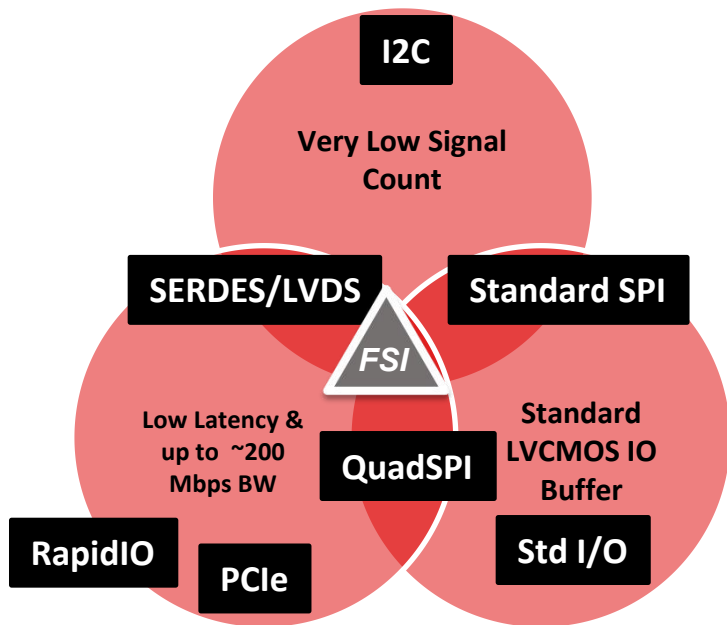
Uniquely meets the three key criteria:
- Very low signal count
- High bandwidth, low latency
- Standard LVCMOS IO buffer

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Fast Serial Interface overview

- Low-latency, high-speed communication
  - Double data rate
  - Minimal packet header and footer

- Built for isolated control topologies
  - Uni-directional signals
  - Single or double data lines

- Robust
  - 8-bit Hardware CRC
  - Line break detection
  - Skew compensation

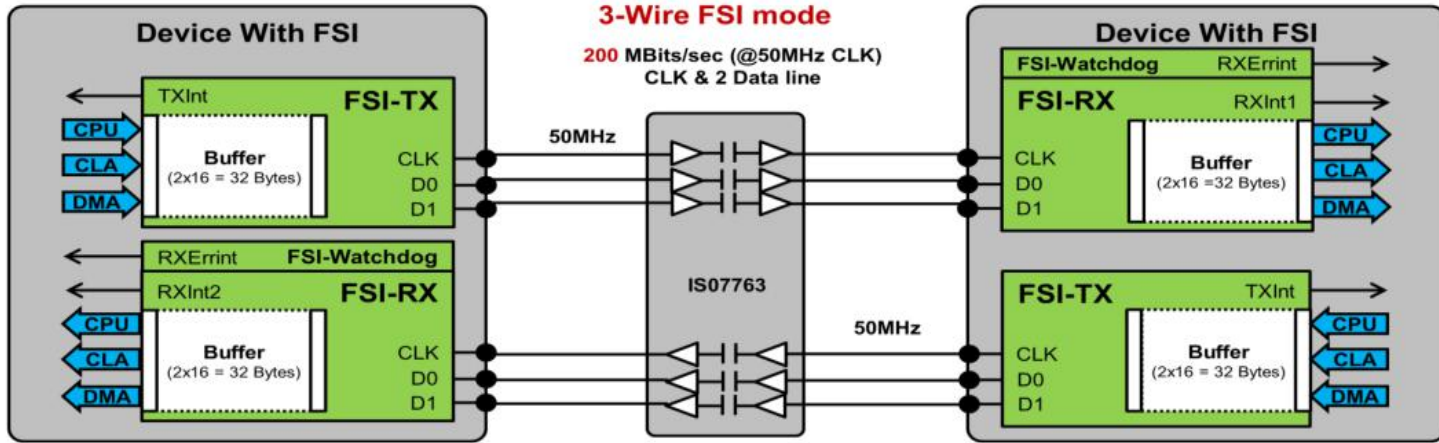- Flexible Topologies
  - Point-to-point
  - Star
  - Daisy chain
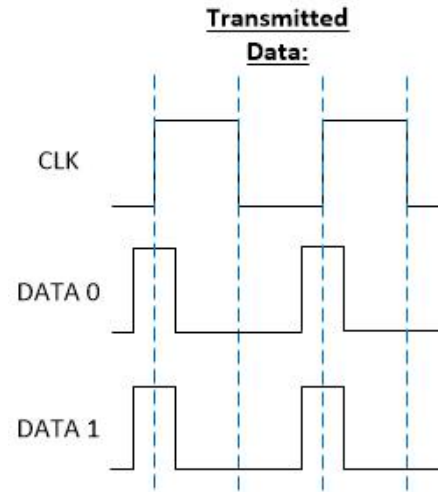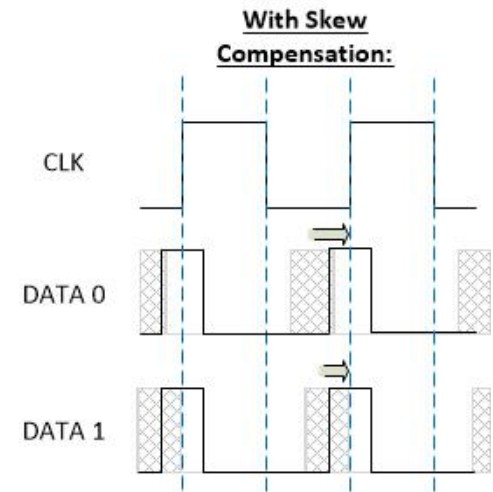
Fast Serial Interface overview

- 100 Mbps - 200 Mbps (1-2 data lines)
- Ideal for Isolation; 4-6 unidirectional signals
- Full-duplex communication
- No fixed master and slave structure
- Flexible topologies

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# TMDSFSIADAPEVM

Features

Solution scope

- System
    - Validates the FSI link and system capabilities
    - Enables isolated control topologies
- Hardware
    - Adapter board to enable C2000 MCU development
    - Compatible with all FSI enabled EVMs
        - Works in conjunction with BoosterPacks and controlCARDs
    - Supports LVDS (100/200) Mbps
    - Supports RS485 (100Mbps)
    - Uses standard Cat-5 Cable
- Software
    - SW example fast data transfer across isolation links
    - Examples in C2000Ware

Applications

- Distributed control architectures
- Servo Drives
- Grid Infrastructure
- Low cost fast serial network for automation
- Enables low cost peripheral expansion and smart sensing applications

Benefits

- High-speed allowing more data, fewer channels required, and distributed control architectures
- Low channel count to reduce cost of isolation

http://www.ti.com.cn/cn/lit/ug/swru555/swru555.pdf

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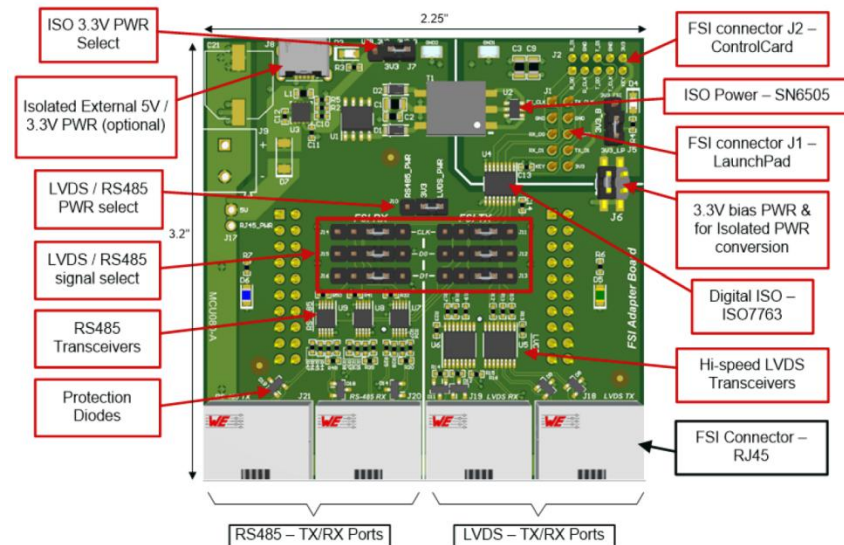
TIDM-02006 – *Distributed multi-axis servo drive over Fast Serial Interface (FSI)*

Features

- Demonstrate high-speed (100mbps) communication using fast serial interface (FSI) for real-time control
- Implement position and velocity control loops for all slave axes on F2838x based master node, torque/current loops on F28004x based slave nodes
- Up to 16 axes. Simultaneous start and stop control. Low latency (high bandwidth) and precision control of distributed multi-axis servo drive system
  - 1uS/2uS sampling to PWM latency with F2838x/F28004x respectively
  - <2uS command jitter among slave nodes
- Leverage F2838x's multi-cores. Speed and position control over FSI for all slave nodes on CPU1, Main axis control on CPU2, EtherCAT communication with host PC on CM.
- Integrated SFRA tool on both F28004x and F2838x to support speed and current loop tuning
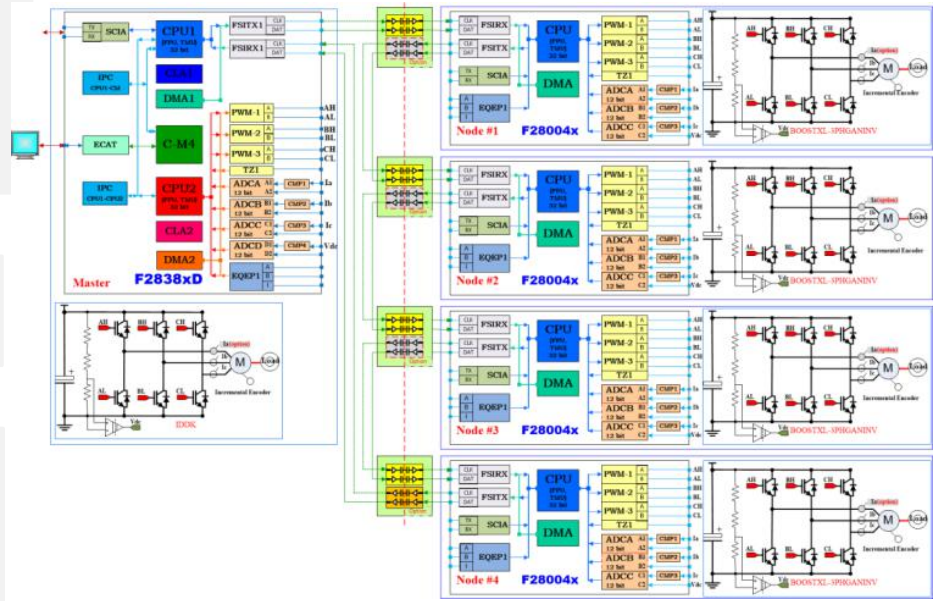
Target Applications

- Industrial servo drives
- Factory automation and control
- Robotics

Tools & Resources

- **TIDM-02006**
- **Design Guide**
- **Design Files:** Design Files, Software
- **Key TI Device:**
  - TMS320F280049C → TMS320F280025C
  - TMS320F28388D

- **Development Boards:**
  - TMDXIDDK379D
  - TMDSCNCD28388D
  - LAUNCHXL-F280049C
  - BOOSTXL-3PHGANINV
  - TMDSFSIADAPEVM

Benefits

- High control performance , high-speed communication with low jitter, and ease of use
- Easy to tune control loops using SFRA tool
- Reduced system cost (fewer isolated channels) and increased reliability due to fast serial interface (FSI)
- Reduced development time due to built-in incremental software build levels

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C2000™ peripheral deep dive:
Defy conventional logic with customizable on-chip peripherals

Configurable Logic Block (CLB)

Integrate custom logic and *augment* peripheral capability in your real-time MCU applications

Customized logic is usually done in a system by adding FPGAs, CPLDs, or external logic. These systems almost always still include a traditional microcontroller as well.

Scenario without CLB

MCU → FPGA CPLD External logic
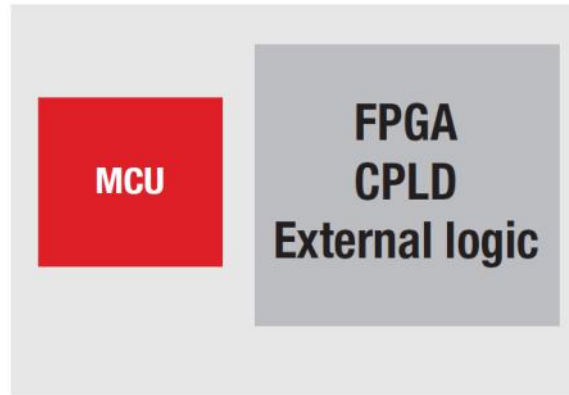
With CLB

C2000 MCU
CLB

C2000 Configurable Logic Block (CLB) enables customization in a microcontroller based real-time control system while eliminating or reducing the size of the FPGA, CPLD, or external logic

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What can be done with the CLB?

- Advanced PWM protection schemes for reliability and safety
- Complex PWM generation, burst mode PWM, and periodic blanking
- Complex signal capture and sequence detection
- Logic based filters and signal conditioning
- Task profiling and time threshold monitoring
- Highly customized general purpose outputs
- Pulse train outputs
- Absolute encoder interfaces
- What can you imagine?
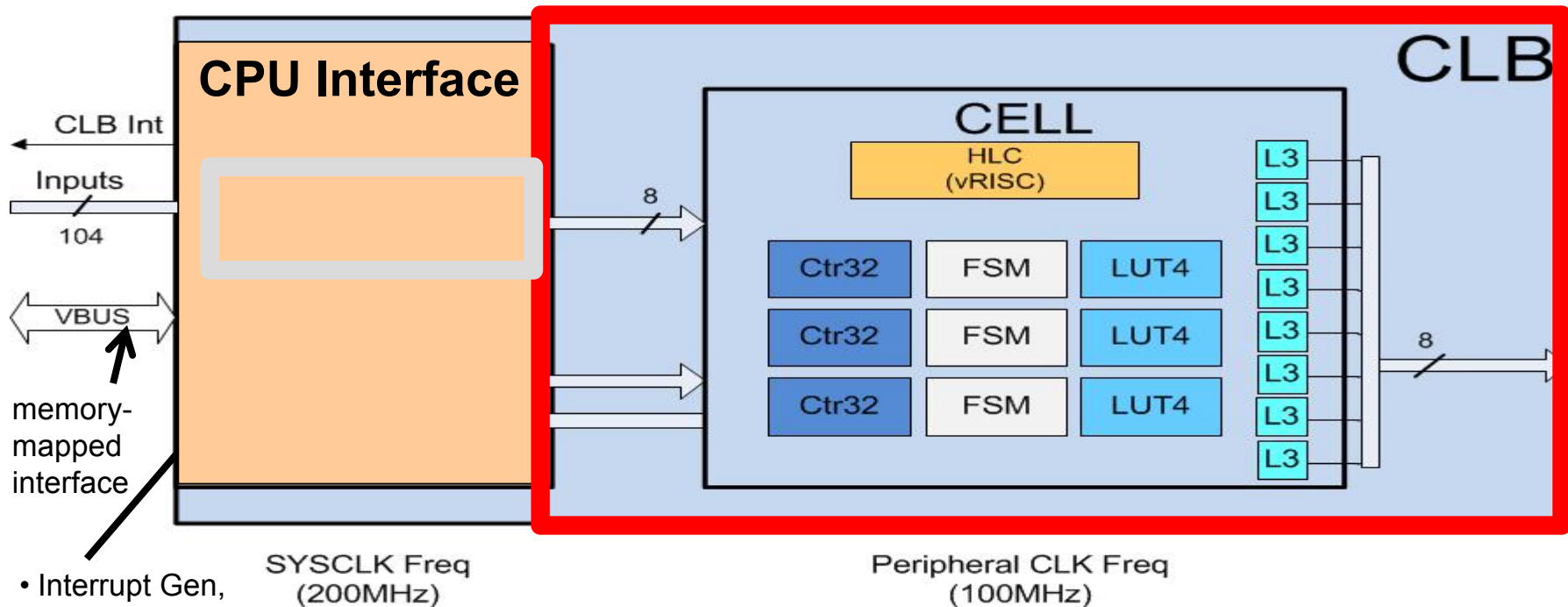
TEXAS INSTRUMENTS

C2000 configurable logic block peripheral
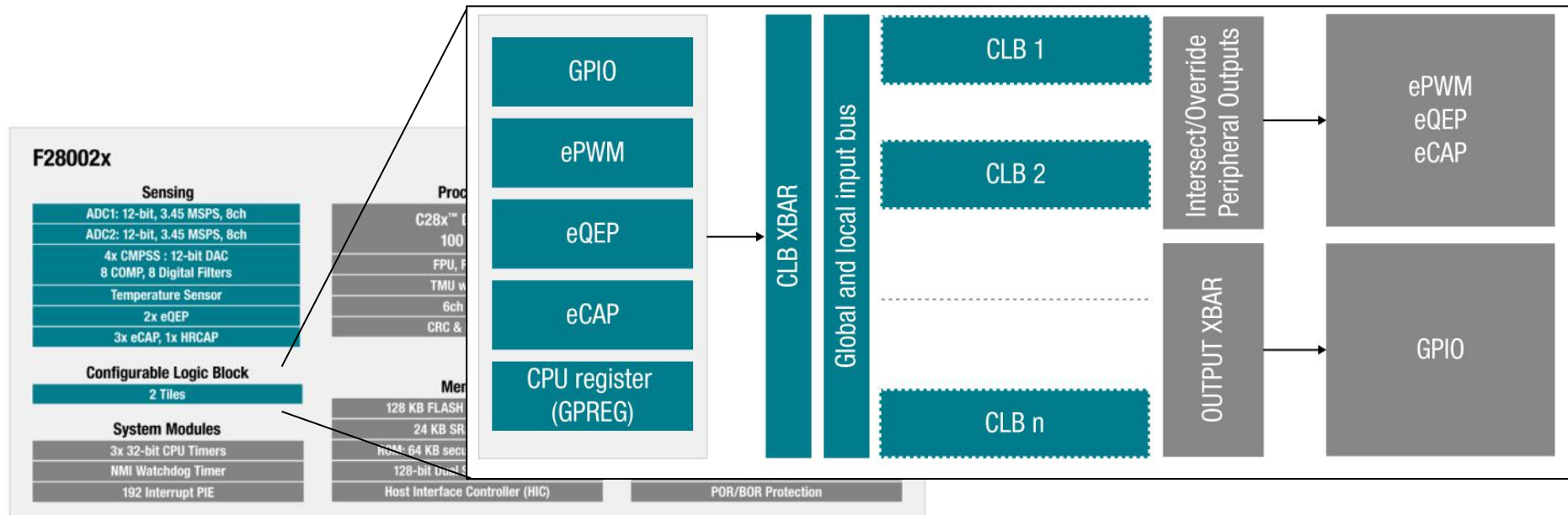
Configurable Logic Block gives the ability to:

- Build logic around and augment existing on-chip peripherals like ePWM, eCAP, eQEP, and GPIOs

- Implement independent custom logic

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CLB structure

CPU Interface

CLB Int

Inputs
104

VBUS

memory-
mapped
interface

• Interrupt Gen,
• Data Exchange
• Programmation

SYSCLK Freq
(200MHz)

CLB

CELL

HLC
(vRISC)

Ctr32   FSM   LUT4
Ctr32   FSM   LUT4
Ctr32   FSM   LUT4

L3 L3 L3 L3 L3 L3 L3 L3 L3 L3

8

8

Peripheral CLK Freq
(100MHz)

L3: OUTLUT(0-7) (3-inputs, 1-output)
LUT4: LUT(0-2) (4-inputs, 1-output)
FSM: FSM(0-2) Finite state machine
Ctr32: CNT(0-2) Counter module
HLC: High level controller

TEXAS INSTRUMENTS

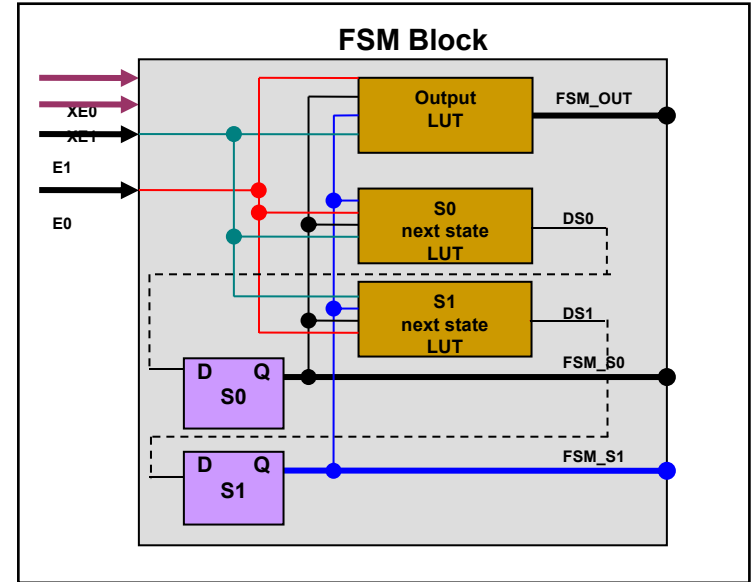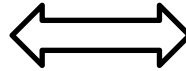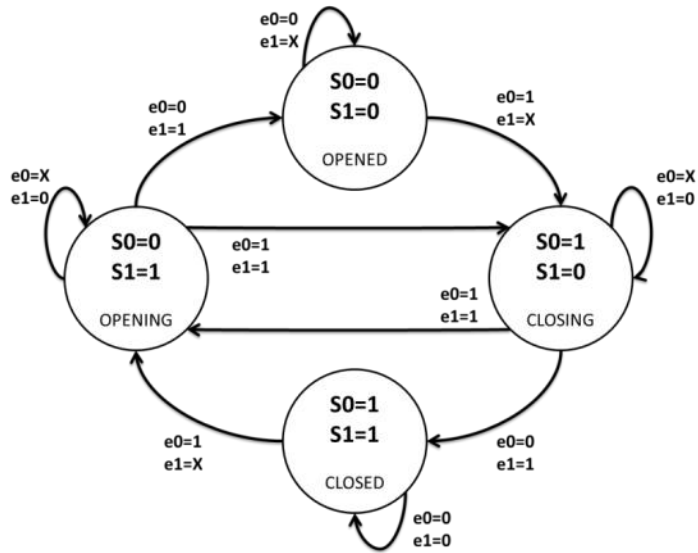# 4-input LUT (LUT4)

- **L**ook **U**p **T**able
- 4 inputs and one output
- **Any function of 4 inputs** (or less) can be realized.
- C syntax

4 input AND	O = i1 & i2 & i3 & i0
3 input OR	O = i1 | i2 | i0
More complex	O = (!i2 & (i1 | i0))

i0
i1
i2
i3

Any combinational function of upto 4 inputs can be realized by this block.
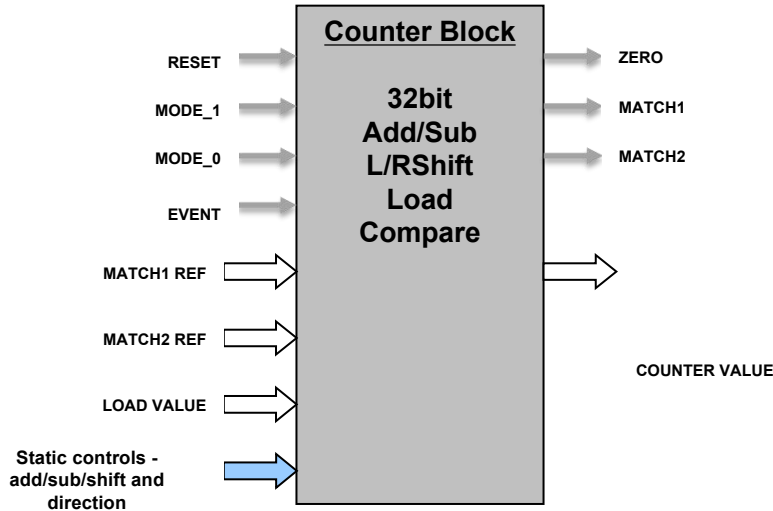
Q
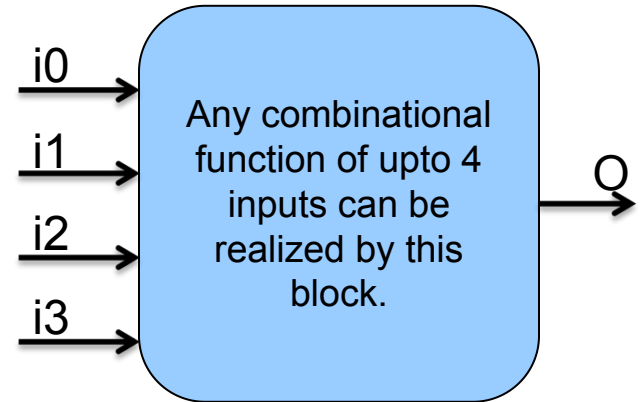
FSM

- Allows implementing **Finite State Machines (FSM)** of up to 4 states
  - One 4-state FSM or Two 2-state FSMs
- E0 and E1: Two inputs control FSM_OUT or either of the states S0 and S1.
- S0 and S1 are two state bits that have independent state control equations.

Counter block

Counter Block

32bit
Add/Sub
L/RShift
Load
Compare

RESET
MODE_1
MODE_0
EVENT
MATCH1 REF
MATCH2 REF
LOAD VALUE
Static controls - add/sub/shift and direction

ZERO
MATCH1
MATCH2

COUNTER VALUE

If reset = 1 — yes → Reset counter to 0

no

If event = 1 — yes → Load/add/sub/shift based on setting

no

COUNT

Count up if mode1 = 1, else count down

mode_0 acts as an enable

Yes ← mode_0=1

Inputs

- **RESET** : If high, reset to 0 on the next clock cycle.
- **MODE_0** : counting operation only when this input is high.
- **MODE_1** : High → Increment, Low → Decrement
- **EVENT** : Load, Right/Left shift, Add/subtract predefined value
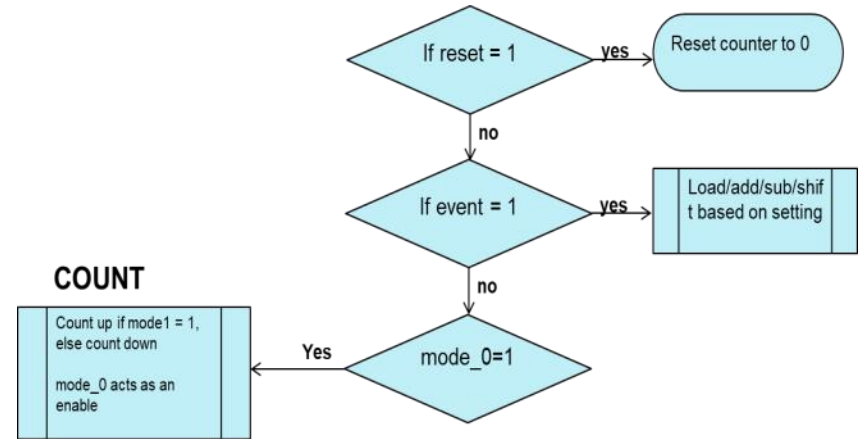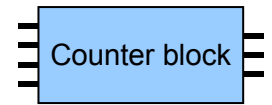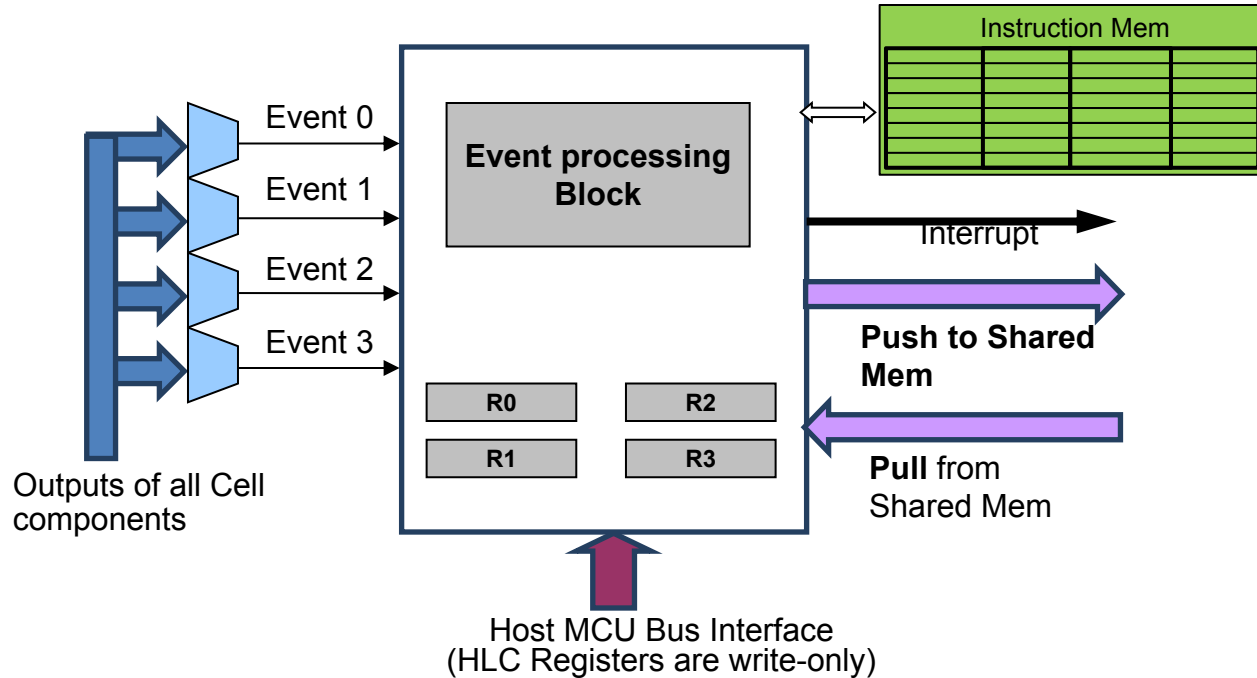
Outputs

- **ZERO** : High when counter value is 0.
- **MATCH1** : High when counter value equals MATCH1
- **MATCH2** : High when counter value equals MATCH2

TEXAS INSTRUMENTS

HLC architecture
(high-level-controller)

HLC

Instruction Mem

HLC Instructions

- Mov <src>,<dst>
- Mov_T1 <src>,<dst>
- Mov_T2 <src>,<dst>
- ADD   <src>,<dst>
- Sub   <src>,<dst>
- PUSH <src>
- PULL <src>
- INTR <const:6>

Where <src/dst> =

- R0-R3 (HLC Regs)
- C0-C2 (Counter values)

Event 0

Event 1

Event 2

Event 3

Event processing Block

R0   R2

R1   R3

Interrupt

Push to Shared Mem

Pull from Shared Mem

Outputs of all Cell components

Host MCU Bus Interface
(HLC Registers are write-only)

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CLB advantages vs FPGA and CPLD

- Integrated into a high-performance fully programmable real-time controller

- Residing inside the C2000 MCU, the CLB has direct access to key CPU and peripheral signals

- Internal signals can be used to supplement or modify logic inside control peripherals and external glue logic

- The simple programmable processor (HLC) facilitates data transfers between CLB and CPU memory. Up to four stored programs can be triggered by low-to-high transition of selected internal CLB signals.

- Timing of CLB signals already designed for the specified CPU frequency; any logic that is created using CLB is guaranteed to meet the timing requirements

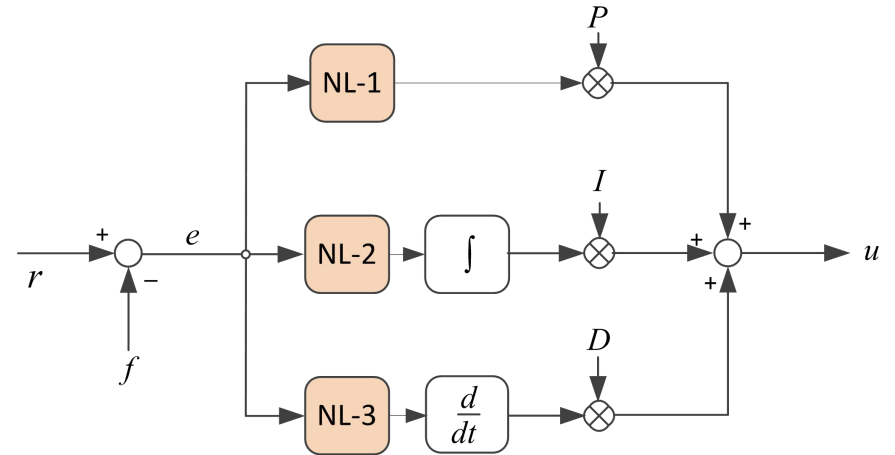- Fully software configurable and can be changed easily in-system

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C2000 Digital Control Library

Nonlinear PID Overview

TEXAS INSTRUMENTS
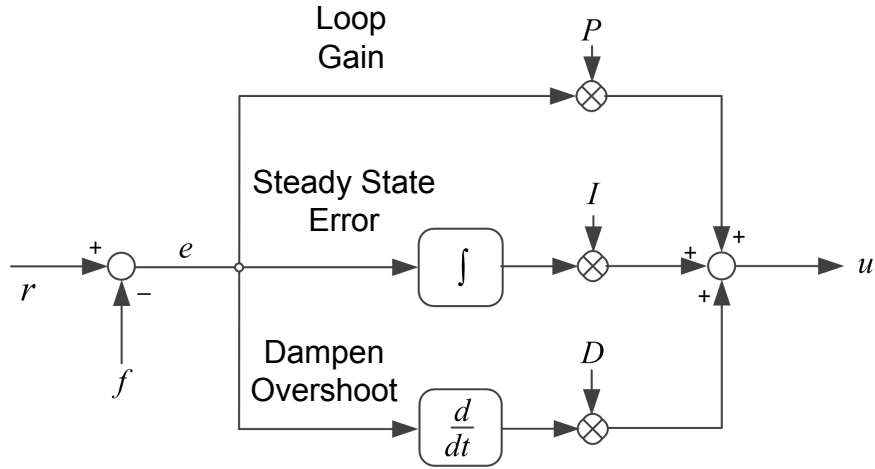
Nonlinear PID

Classical PID Control

Non-linear PID – Current State-of-the-art

TEXAS INSTRUMENTS

# NLPID system-level benefits (on F28002x and beyond)

- **Improved of control performance - up to 4x faster transient response**
  - Without need to increase sampling/switching frequency (thanks to enhanced instructions in the TMU accelerator)
  - Without need of higher MHz CPU, ultimately saving cost (don't need expensive processor, data converters, etc) and making the most out of available MIPS
  - Especially beneficial for timing critical applications that demand a fast transient response, like server and telecom power and motor control

- **Simpler tuning process compared to Look-Up-Tables**
  - Single tunable parameter in each path - gain scheduling not necessary for NLPID

- **Better disturbance rejection and regulation control**
  - Saves processing power
  - Improved speed + position control in servo applications
  - Improved voltage regulation in power supply applications

What Comes in the Box?

C2000Ware or controlSUITE™ Software Suite

Code Composer Studio™ (CCS) IDE
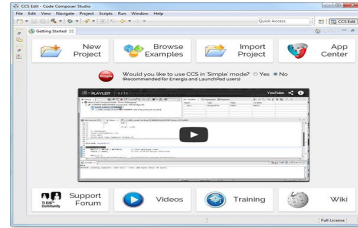
Hardware Development Kits

Application Expertise

http://www.ti.com/c2000

Training and Support

3rd Party Innovation and Support

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- 可订购预发布产品，快人一步

便利直达

支持人民币价格显示和交易结算，可免报关

支付方式多样化：
支付宝、微信支付、银联个人和企业网银支付

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Thank you!

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