MSPM0 DMA module introduction

MSPM0 peripheral training series

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## MCU level overview

### MSPM0Lxx series

- **CPU**: Arm Cortex-M0+, 32 MHz
- **NVIC**: 3-ch DMA
- **On-chip Memory**: 8, 16, 32 or 64 kB flash, 2 or 4 kB SRAM
- **Data Integrity & Security**: CRC accelerator (16 and 32 bit)
- **Programming & Debug**: ARM SWD interface, UART & I2C bootloader

**Power & Clocking**
- POR / BOR / SVS
- Internal LF 32kHz (3%)
- Internal HF 4-32MHz (1%)

**Communication**
- UART w/ LIN (1)
- UART (1)
- SPI (1)
- I2C (2) w/ FastMode+

**Analog**
- 12-bit ADC 1.45Msps (10-ch)
- Comparator w/ 8-bit DAC
- General purpose amp
- Internal ADC reference (1.5%)

**Timers**
- Low power 16-bit 2 CC (4)
- Windowed watchdog

**IO**
- Up to 28 GPIO
- Up to 2 low tbl CPA inputs

#### 32 MHz MCU with up to 64kB flash, 32 pins, 12-bit ADC, dual zero-drift OPA/PGA, COMP

### MSPM0Gxx series

- **CPU**: Arm Cortex-M0+, 80 MHz
- **NVIC**: MPU/OPU, 7-ch DMA
- **On-chip Memory**: 32, 64, or 128 kB flash [ECC], 16 or 32 kB SRAM [ECC]
- **Data Integrity & Security**: CRC accelerator (16 and 32 bit), AES256 accelerator + TRNG
- **Programming & Debug**: ARM SWD interface, UART & I2C bootloader

**Power & Clocking**
- POR / BOR / SVS
- External LF 32kHz XTL
- External HF 4-48MHz XTL
- Internal LF 32kHz (3%)
- Internal HF 4-32MHz (1%)

**Communication**
- UART w/ LIN (1)
- UART (3)
- SPI (2)
- I2C (2) w/ FastMode+

**Analog**
- 12-bit ADC 4Msps (9-ch)
- External LF 32kHz XTL
- External HF 4-48MHz XTL
- Advanced control 16-bit 2 CC (1)
- General purpose 32-bit 2 CC (1)
- Low power 16-bit 2 CC (2)
- Real-time clock (1)

**Timers**
- Advanced control 16-bit 2 CC (1)
- General purpose 32-bit 2 CC (1)
- General purpose 16-bit 2 CC (2)

#### 80 MHz MCU with up to 128kB flash, 64 pins, advanced analog, AES/TRNG, CAN-FD
MSPM0 DMA module introduction

Key features

- Up to sixteen independent transfer channels
- MSPM0G350x MCUs have 7 DMA channels and MSPM0Lxx MCUs have 3 DMA channels
- Configurable DMA channel priorities
- Byte, short word, word and long word or mixed byte and word transfer capability
- Transfer counter block size supports up to 64k transfers of any data type
- Configurable DMA transfer trigger selection
- Six flexible addressing modes
  1. Fixed address to fixed address
  2. Fixed address to block of addresser
  3. Block of addresser to fixed address
  4. Block of address to block of addresser
  5. Fill data to block of address
  6. Data table to specific address
- Single or block transfer modes
- Repeated transfer modes
DMA addressing modes

1. **Fixed Address To Fixed Address**
   - DMA Controller
   - Address Space
   - Fixed Address
   - Address Space

2. **Fixed Addresses To Block Of Addresses**
   - DMA Controller
   - Address Space
   - Fixed Addresses
   - Block Of Addresses

3. **Block Of Addresses To Fixed Address**
   - DMA Controller
   - Address Space
   - Block Of Addresses
   - Fixed Address

4. **Block Of Addresses To Block Of Addresses**
   - DMA Controller
   - Address Space
   - Block Of Addresses
   - Block Of Addresses

5. **Fill Data To Block Of Addresses**
   - DMA Controller
   - Address Space
   - Fill Data
   - Block Of Addresses

6. **Data Table To Specific Address**
   - DMA Controller
   - Address Space
   - Data Table
   - Specific Address
DMA module quick start

Academy
DMA introduction lab

Driverlib Examples
MSPM0G350x:
- dma_block_transfer
- dma_file_data
- dma_table_transfer

MSPM0L13xx:
- dma_block_transfer
- dma_file_data
- dma_table_transfer

Related Links
MSPM0 online resource
MSPM0 quick start guide
MSPM0 Sysconfig user’s guide
MSPM0G350x datasheet
MSPM0L13xx datasheet
MSPM0Gxx technical reference manual
MSPM0Lxx technical reference manual

Launchpad
LP-MSPM0G3507
LP-MSPM0L1306

Sysconfig Entrance for DMA Setting

Related Links
Launchpad
LP-MSPM0G3507
LP-MSPM0L1306
To find more MSPM0 training series, please visit:

- TI.com.cn
- WeChat (德州仪器公众号)
- Bilibili
- 21IC