

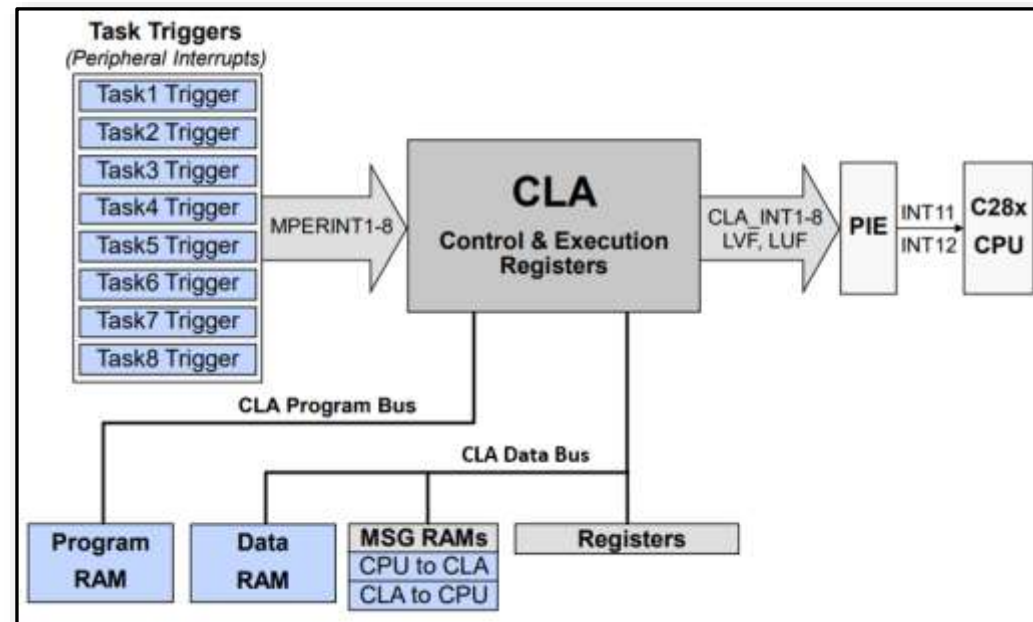
F28P55x编程实例Labs-CLA

- **Code Composer Studio**
- **C2000Ware**
- **LaunchXL-F28P55x**

CLA

Control Law Accelerator , 控制率加速器

- 32位浮点数字处理单元 · FPU
- 平行于CPU, 时钟频率同CPU
- 执行算法和周期性的计算工作
- Type2型, 直接读取ADC结果寄存器
- 直接操作EPWM、ECAP、EQEP、PGA等数据寄存器
- 独立响应外设中断



Type	Description	Devices Covered	Device-Specific Options
0	Original CLA Module Type	2803x	Only supports data RAM0 and 1 and does not allow CPU access when CLA data RAM is enabled.
		2805x, 2806x	Adds supports for data RAM2 and adds option to enable CPU access to data RAMs.
1	Increased Program address reachability to 16-bits; added instructions to support the new address reach; added two new offset addressing modes; CLA program memory is now user selectable and can reside anywhere in the lower 64k address space (excluding the M0 and M1 space). The job of giving control to the CLA and assigning triggers to a task is now done at the system level; a task can now fire an interrupt to main CPU mid execution.	2807x, 2837xD, 2837xB	—
2	Added Background-code mode, that can run task like communications and clean-up routines in Background; Background tasks runs continuously until disable or device/soft reset; Background task can be triggered by a peripheral or software; other foreground tasks can interrupt background task in the priority order defined; added provision for making sections of background code uninterruptible; added debug enhancements that has true software breakpoint support, where CLA re-fetches from the same address where halted during debug stop.	28003x, 28004x, 2836x, 28P55x, 28P65x	—

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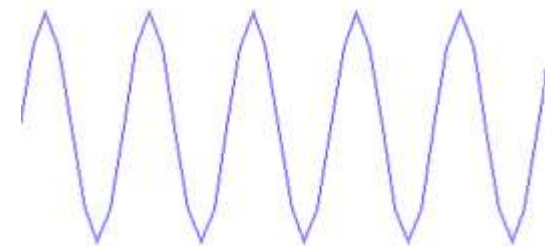
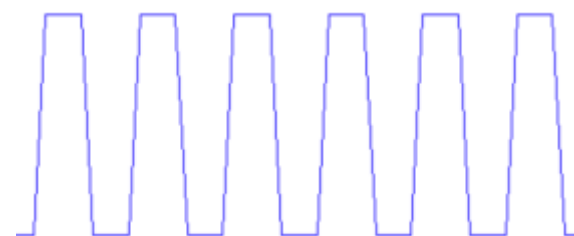
功能实现

用CLA实现一个FIR低通滤波器，方波输入，正弦波输出，EPWM1产生方波，ADC采样方波，EPWM2用于ADC的采样触发。

实现步骤

- 复制空白工程
- Sysconfig配置GPIO
- Sysconfig配置EPWM1
- Sysconfig配置EPWM2
- Sysconfig配置ADC
- Sysconfig配置CLA

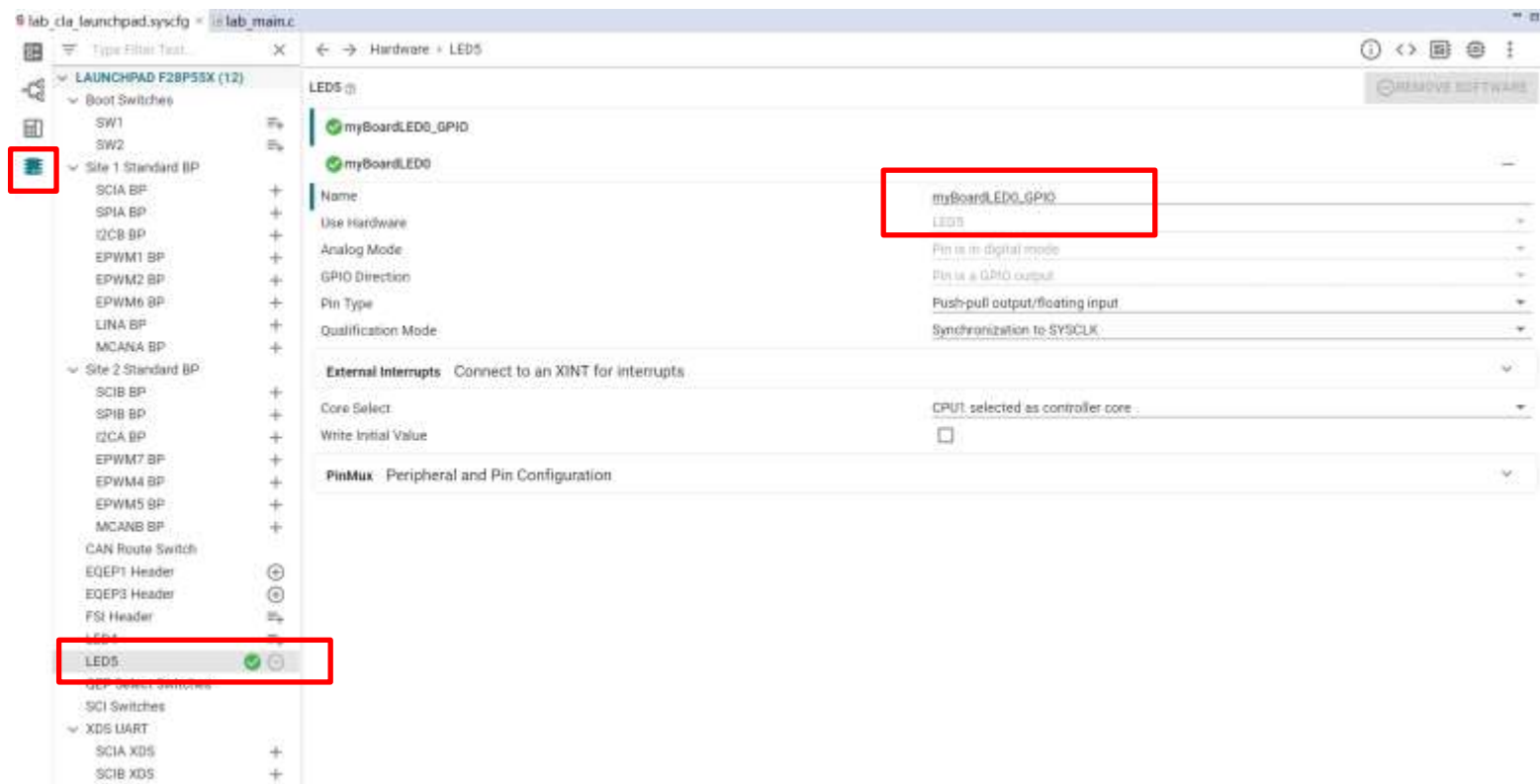
- 编写应用代码



片上资源	PIN脚	用途
myBoardLED0_GPIO	LED5	指示系统的运行
EPWM1	--	产生PWM
EPWM2	--	触发ADC
ADCINA0		用于AD采样
CLA	--	配置CLA

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$$\text{Time Base Period} = \frac{f_{tbclk}}{2f_{pwm}} = \frac{100 \times 10^6}{2 \times 1000} = 50000.$$

$$\text{Counter Compare Value} = \left(1 - \frac{\text{duty}}{100}\right) * \text{tbprd} = \left(1 - \frac{50}{100}\right) * 50000 = 25000.$$

The screenshot shows the TI Studio configuration window for an EPWM module. The left sidebar lists various system components, with 'EPWM' selected and highlighted in a red box. The main configuration area is divided into two sections: 'EPWM Time Base' and 'EPWM Counter Compare'. In the 'EPWM Time Base' section, the 'Time Base Period' is set to 50000, and the 'Counter Mode' is set to 'Up-down-count mode', both highlighted with red boxes. In the 'EPWM Counter Compare' section, the 'Counter Compare A (CMPA)' value is set to 25000, also highlighted with a red box.

CLA

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The screenshot shows the TI Configurator interface for configuring an EPWM module. The left sidebar displays a system tree with various components, and 'EPWM' is selected under the 'CONTROL (5)' category. The main configuration area is titled 'EPWM Action Qualifier' and includes several sections:

- EPWMA Action Qualifier:** Includes options for 'Enable Continuous SW Force Global Load' (disabled), 'Continuous SW Force Shadow Mode' (disabled), and 'T1/T2 Trigger Source'.
- ePWMxA Output Configuration:** Includes 'ePWMxA Global Load Enable' (disabled), 'ePWMxA Shadow Mode Enable' (checked), 'ePWMxA Shadow Load Event' (set to 'Load when counter equals period'), 'ePWMxA One-Time SW Force Action' (set to 'No change in the output pins'), and 'ePWMxA Continuous SW Force Action' (set to 'Software forcing disabled').
- ePWMxA Event Output Configuration:** Lists various events and their corresponding actions. The actions 'Set output pins to High' and 'Set output pins to low' are highlighted with a red box.

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ADCINA0		用于AD采样
CLA	--	配置CLA

The screenshot shows the TI Configurator interface. On the left, a tree view lists various system components. The 'EPWM' component under the 'CONTROL' category is highlighted with a red box. On the right, the configuration panel for EPWM1 is displayed. A red box highlights the 'PinMux' section, showing the following configuration:

- EPWM1
- GPIO0/79 (EPWM1 BP)
- GPIO1/78 (EPWM1 BP)

Both GPIO pins are marked as 'Connected to hardware (Un-suppress)'.

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$$\text{Time Base Period} = \frac{f_{tbclk}}{f_{pwm}} - 1 = \frac{100 \times 10^6}{8000} - 1 = 12499.$$

CLA

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myBoardLED0_GPIO	LED5	指示系统的运行
EPWM1	--	产生PWM
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CLA	--	配置CLA

lab_cla_launchpad.syscfg x lab_main.c

SYSTEM (18)

- AIO
- CLA 1/1
- CLB INPUTXBAR INPUT
- CLB OUTPUTXBAR
- CLBXBAR
- CPUTIMER
- DCC
- EPWMXBAR
- ERAD
- FLASH
- GPIO 1/00
- INPUTXBAR INPUT
- INTERRUPT 1
- MEMCFG 1/1
- OTHER
- OUTPUTXBAR
- SYSTCL
- WATCHDOG

ANALOG (6)

- ADC 1/3
- ANALOG PinMux 1/1
- ASYSCTL 1/1
- DMPSS
- DAC
- PGA

CONTROL (5)

- CLB
- ECAP
- EPWM 2/12**
- EQEP
- SYNC 1/1

COMMUNICATION (10)

- DMA
- FSRX
- FSITX
- I2C
- LIN
- MCAN

EPWM2

EPWM Dead-Band

EPWM Chopper

EPWM Trip Zone

EPWM Digital Compare

EPWM Event-Trigger

Enable EPWM Interrupt

ADC SOC Trigger

SOCA Trigger Enable

SOCA Trigger Source Time-base counter equal to period

SOCA Trigger Event Count 1 Event Generates Interrupt

SOCA Trigger Event Count Initial Value Load Enable

SOCB Trigger Enable

HRPWM

PinMux Use Case ALL

PinMux Qualification

PinMux Peripheral and Pin Configuration

EPWM Peripheral

EPWM_A

EPWM_B

EPWM2

GPIO2/77 (EPWM2 BP)

Connected to hardware(Un-suppress)

GPIO3/76 (EPWM2 BP)

Connected to hardware(Un-suppress)

CLA

片上资源	PIN脚	用途
myBoardLED0_G PIO	LED5	指示系统的运行
EPWM1	--	产生PWM
EPWM2	--	触发ADC
ADCINA0	--	用于AD采样
CLA	--	配置CLA

The screenshot displays the TI Studio configuration environment for an ADC. The left sidebar shows the component tree with 'ADC' selected under 'ANALOG (5)'. The main configuration area is titled 'ADC (1 of 5 Added)' and shows the configuration for 'myADC0'. The right-hand pane contains several sections with red boxes highlighting specific values:

- Name:** myADC0
- ADC Instance:** ADCA
- ADC Clock Prescaler:** ADCCLK + (input clock) / 4.0
- SOC Configurations:** Start of Conversion Configurations
- Enable SOC0:** SOC0 Start of Conversion 0
- SOC0 Name:** SOC0
- SOC0 Channel:** single-ended, ADCINA0
- SOC Triggers:** Trigger Mode: Single Trigger; SOC0 Trigger: ePWM2, ADCSOCA
- Sample Time Calculator:** SOC0 Sample Window [SYSCLK counts]: 8

CLA

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EPWM1	--	产生PWM
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ADCINA0		用于AD采样
CLA	--	配置CLA

lab_cla_launchpad.syscfg x lab_main.c

Software + ADC

SOC0 Sample Window [SYSCLK counts]

SOC0 Sample Time [ns]

ADC Repeater Module

ADC INT Configurations Interrupt Configurations

ADC interrupt Pulse Mode

Enable ADC interrupts

INT1 ADC Interrupt 1

Enable ADC Interrupt 1

Interrupt 1 SOC Source

Continuous Interrupt Mode

PPB Configurations Post Processing Blocks Configurations

Burst Mode ADC Burst Mode

Register PIE Interrupt Handlers

Use interrupt

Register Interrupts

Analog PinMux

Name

Use Case

Pins Used

PinMux Peripheral and Pin Configuration

ANALOG Peripheral

SOC/EOC0

myANALOGPinMux0

myANALOGPinMux0

CUSTOM

A0, B15, C15, DACA_OUT

Any(ANALOG)

Any(A0, B15, C15, DACA_OUT/23 (Header))

CLA

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CLA	--	配置CLA

The screenshot shows the TI Studio interface for configuring the ASYSCTL module. The left sidebar displays a tree view of system components, with 'ASYSCTL' highlighted in a red box. The main window shows the configuration options for ASYSCTL, including 'Analog Reference' where 'Internal' and '1.65V' are selected, also highlighted in a red box.

ASYSCTL

Temperature Control

Enable Temperature Sensor

Lock Temperature Sensor Control Register

Analog Reference

Analog Reference: Internal

Analog Reference Voltage: 1.65V

External DACL Enable

CMPSS DACL Output Enable

CLA

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The screenshot displays the TI Configurator interface for configuring the CLA (Control Law Accelerator) instance 'myCLA0'. The left sidebar shows a tree of system resources, with 'CLA' highlighted. The main configuration area shows the following settings:

- Name:** myCLA0
- CLA Instance:** CLA1
- CLA Task Configuration:**
 - Enable CLA Task 1:
 - Enable CLA Task 2:
 - Enable CLA Task 3:
 - Enable CLA Task 4:
 - Enable CLA Task 5:
 - Enable CLA Task 6:
 - Enable CLA Task 7:
 - Enable CLA Task 8:
 - Enable CLA Task 9:
- CLA Task 1 Configuration:**
 - Interrupt Vector: CLA_MVECT_1
 - Interrupt Name: Cla1Task1
 - Trigger Source: CLA Task Trigger Source is ADCA1
- C28 Interrupt Register for CLA Task:**
 - Register Interrupt for CLA Task 1:
 - Register Interrupt for CLA Task 2:
 - Register Interrupt for CLA Task 3:
 - Register Interrupt for CLA Task 4:
 - Register Interrupt for CLA Task 5:
 - Register Interrupt for CLA Task 6:
 - Register Interrupt for CLA Task 7:
 - Register Interrupt for CLA Task 8:
- C28 Interrupt Configuration for CLA Task 1:**
 - Name: interrupt_CLA_TASK_1
 - Interrupt Name: INT_myCLA01
 - Interrupt Handler: cla1ISR1
 - Enable interrupt in PIE:

CLA

The screenshot shows the MEMCFG configuration window in TI Studio. The left sidebar lists various components, with MEMCFG selected and highlighted in red. The main window displays the MEMCFG configuration, including RAM Initialization, LSRAM Configuration, Access Protection for RAMs, Lock RAM Config Registers, Access Violation Interrupt, Correctable Error Interrupt, and Register Interrupt Handler. In the LSRAM Configuration section, the 'CPU/CLA shared data memory' option is highlighted with a red box, indicating it is the selected configuration for the CLA program memory.

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