

# MSPM0 CPU module introduction

— MSPM0 peripheral training series

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# MCU level overview

## —MSPM0Lxx series

## —MSPM0Gxx series

### MSPM0L13x3/4/5/6

**CPU**  
ARM Cortex-M0+  
32 MHz

NVIC / 3-ch DMA

**Power & Clocking**

POR / BOR / SVS

Internal LF 32kHz (5%)

Internal HF 4-32MHz (1%)

**Precision**

12-bit SAR

ULP/HS

8-bit reference

Zero-drift

General

Internal

Temperature

**On-chip Memory**

8, 16, 32 or 64 kB flash

2 or 4 kB SRAM

**Communication**

UART w/ LIN (1)

UART (1)

SPI (1)

I2C (2) w/ FastMode+

**Timers**

General

Window

**Data Integrity & Security**

CRC accelerator (16 and 32 bit)

**IO**

Up to 28 GPIO

Up to 2 low Ib OPA inputs

**Programming & Debug**

ARM SWD interface

ROM UART & I2C BSL

Leaded packages: SOT-16, VSSOP-20/28

No-lead packages: WQFN-16, VQFN-24/32

Feature	<a href="#">Cortex-M0</a>	<a href="#">Cortex-M0+</a>	<a href="#">Cortex-M1</a>	<a href="#">Cortex-M23</a>	<a href="#">Cortex-M3</a>	<a href="#">Cortex-M4</a>	<a href="#">Cortex-M33</a>	<a href="#">Cortex-M35P</a>	<a href="#">Cortex-M55</a>	<a href="#">Cortex-M7</a>
Instruction Set Architecture	Armv6-M	Armv6-M	Armv6-M	Armv8-M Baseline	Armv7-M	Armv7-M	Armv8-M Mainline	Armv8-M Mainline	Armv8.1-M Mainline	Armv7-M
TrustZone for Armv8-M	No	No	No	Yes (option)	No	No	Yes (option)	Yes (option)	Yes (option)	No
Digital Signal Processing (DSP) Extension	No	No	No	No	No	Yes	Yes	Yes	Yes	Yes
Hardware Divide	No	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Arm Custom Instructions	No	No	No	No	No	No	Yes	No	Yes	No
Coprocessor Interface	No	No	No	No	No	No	Yes	Yes	Yes	No
DMIPS/MHz*	0.87	0.95	0.8	0.98	1.25	1.25	1.5	1.5	1.6	2.14
CoreMark®/MHz*	2.33	2.46	1.85	2.64	3.34	3.42	4.02	4.02	4.2	5.01
Maximum # External Interrupts	32	32	32	240	240	240	480	480	480	240

32 MHz MCU with up to 64kB flash, 32 ADC, dual zero-drift OPA/PGA, COMP

# MSPM0 CPU module introduction

## Key features

- Arm Cortex-M0+ 32-bit CPU based on ARMv6-M architecture
- 2-stage pipeline
- Internal peripherals(NVIC / SYSTICK / MPU / MTB / Debug interface)
- The smallest footprint and lowest power requirements of all the Cortex-M processors
- The exceptional code density that significantly reduces memory requirements, which maximizes the use of on-chip Flash memory to save memory cost, reduce memory power

## Differences between M0 and M0+

M0+ has 30% less power dissipation, MPU, MTB and fast IO control

## Key differences between G and L MCUs

MSPM0Gxx MCUs have MPU and MTB

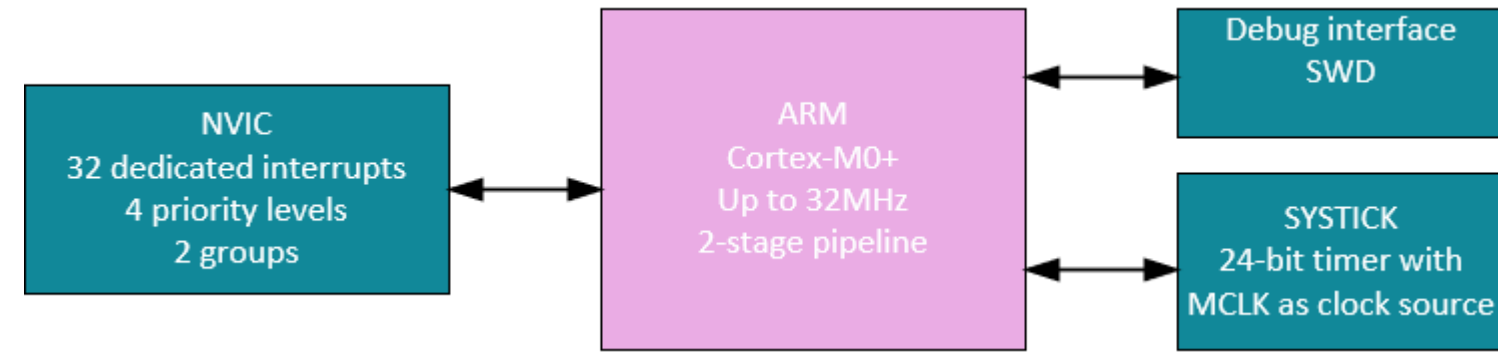


Fig1: MSPM0L CPU Block Diagram

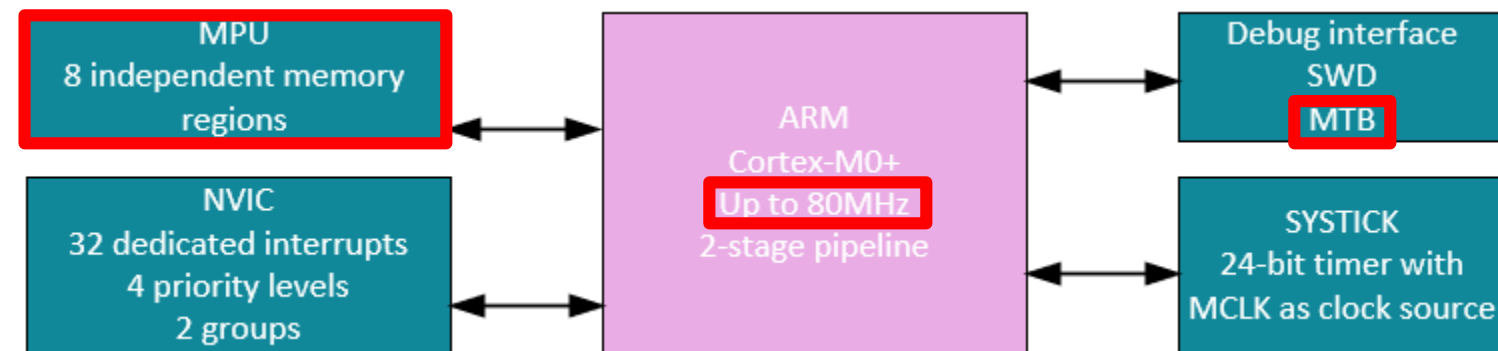


Fig2: MSPM0G CPU Block Diagram

# MSPM0 CPU module in bus organization

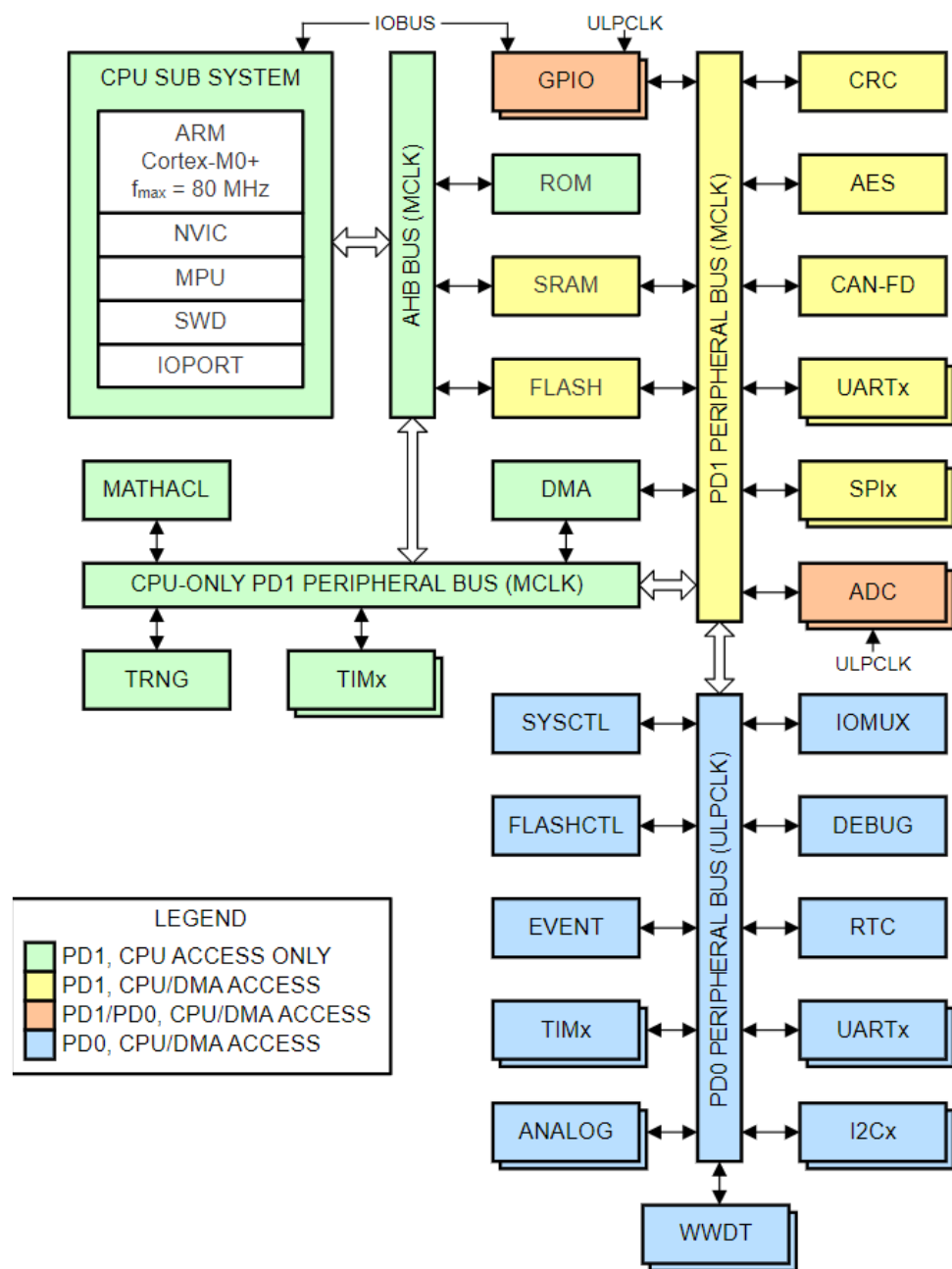


Fig1: MSPM0G Bus organization

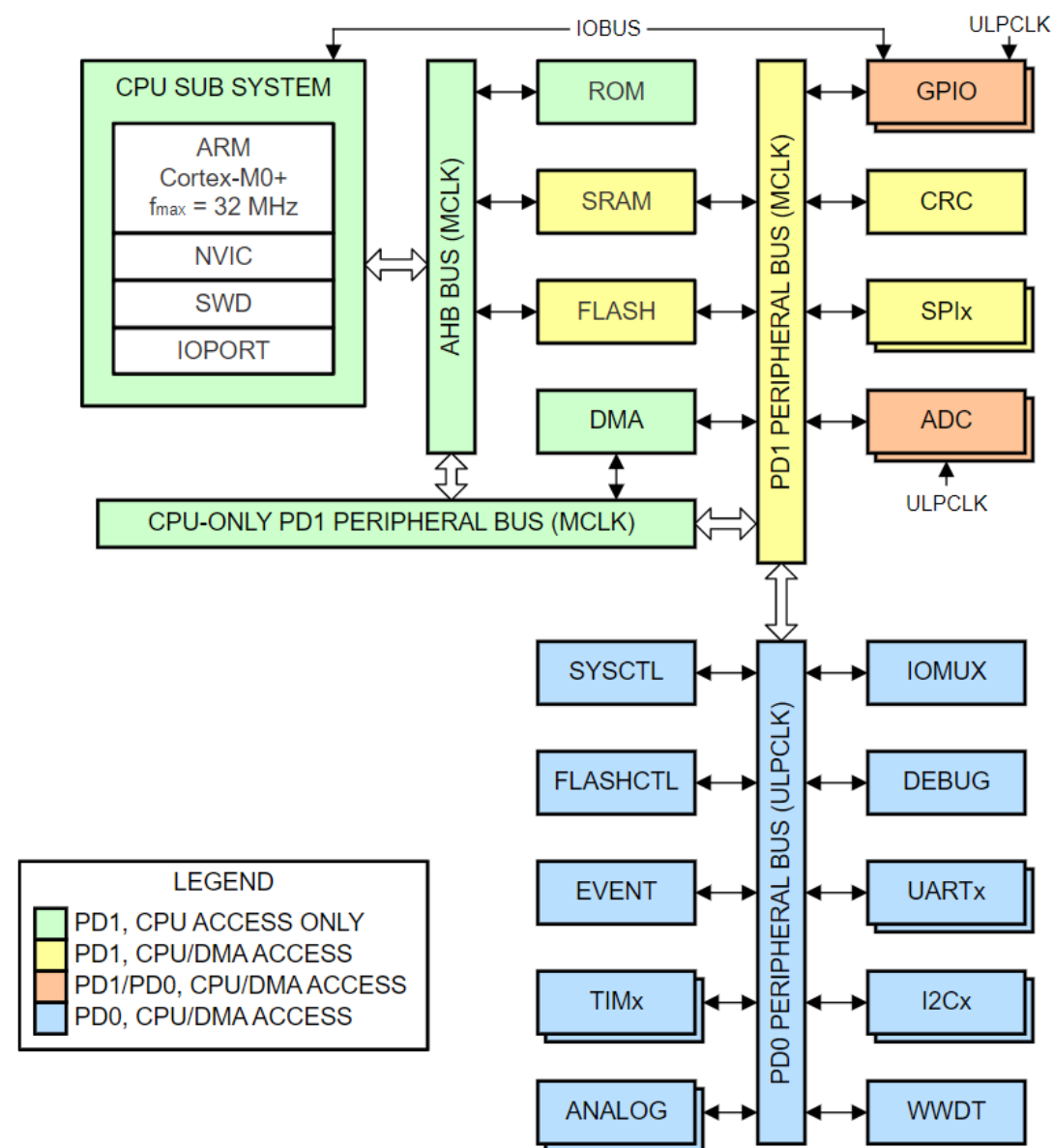


Fig2: MSPM0L Bus organization

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