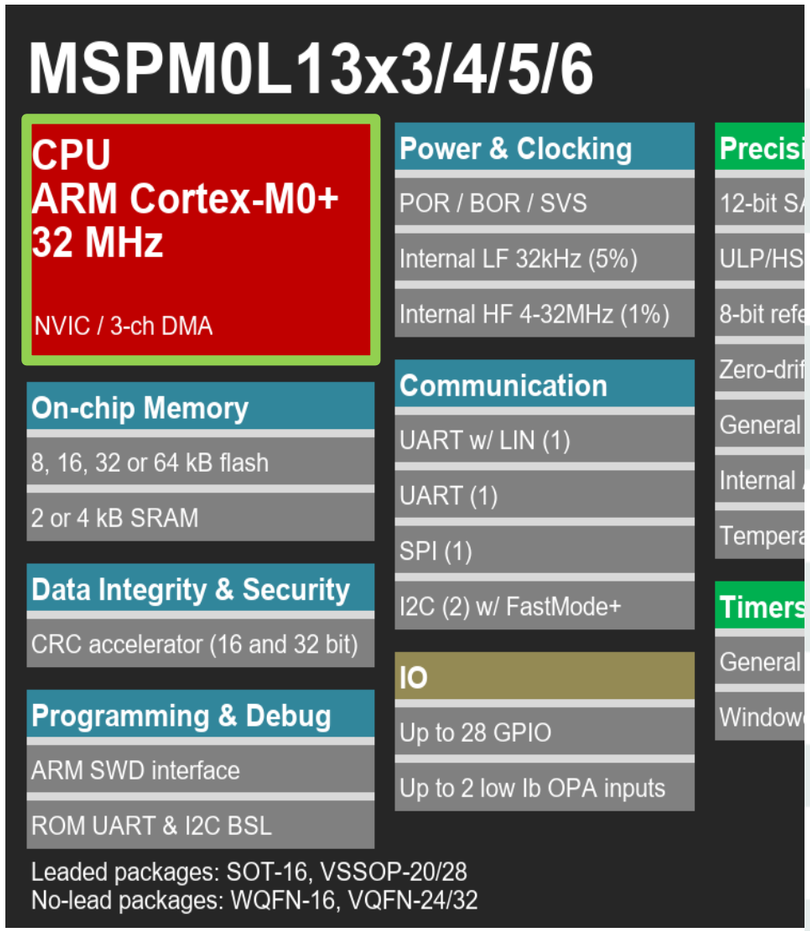
MSPM0 CPU module introduction

—— MSPM0 peripheral training series

Presented by Gary Gao

MCU level overview

——MSPM0Lxx series



32 MHz MCU with up to 64kB flash, 32 ADC, dual zero-drift OPA/PGA, COMP

——MSPM0Gxx series

Feature	Cortex-M0	Cortex-M0+	Cortex-M1	Cortex-M23	Cortex-M3	Cortex-M4	Cortex-M33	Cortex-M35P	Cortex-M55	Cortex-M7
Instruction Set Architecture	Armv6-M	Armv6-M	Armv6-M	Armv8-M Baseline	Armv7-M	Armv7-M	Armv8-M Mainline	Armv8-M Mainline	Armv8.1-M Mainline	Armv7-M
TrustZone for Armv8-M	No	No	No	Yes (option)	No	No	Yes (option)	Yes (option)	Yes (option)	No
Digital Signal Processing (DSP) Extension	No	No	No	No	No	Yes	Yes	Yes	Yes	Yes
Hardware Divide	No	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Arm Custom Instructions	No	No	No	No	No	No	Yes	No	Yes	No
Coprocessor Interface	No	No	No	No	No	No	Yes	Yes	Yes	No
DMIPS/MHz*	0.87	0.95	0.8	0.98	1.25	1.25	1.5	1.5	1.6	2.14
CoreMark®/ MHz*	2.33	2.46	1.85	2.64	3.34	3.42	4.02	4.02	4.2	5.01
Maximum # External Interrupts	32	32	32	240	240	240	480	480	480	240

MSPM0 CPU module introduction

Key features

- Arm Cortex-M0+ 32-bit CPU based on ARMv6-M architecture
- 2-stage pipeline
- Internal peripherals(NVIC / SYSTICK / MPU / MTB / Debug interface)
- The smallest footprint and lowest power requirements of all the Cortex-M processors
- The exceptional code density that significantly reduces memory requirements, which maximizes the use of on-chip Flash memory to save memory cost, reduce memory power

Differences between M0 and M0+

M0+ has 30% less power dissipation, MPU, MTB and fast IO control

Key differences between G and L MCUs

MSPM0Gxx MCUs have MPU and MTB

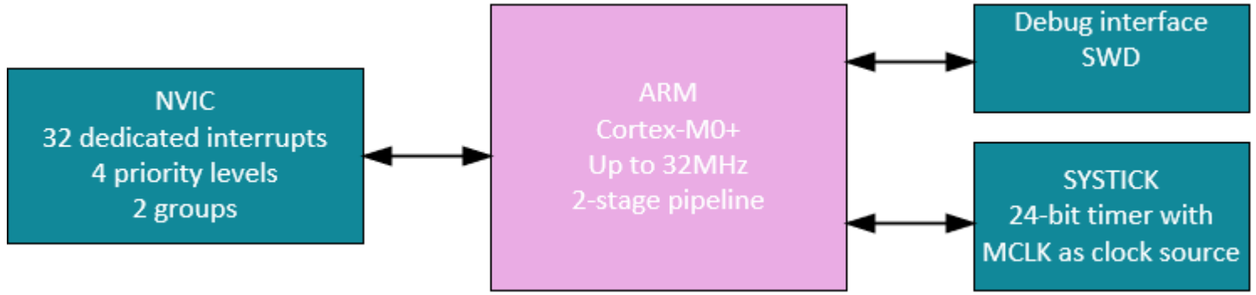


Fig1: MSPM0L CPU Block Diagram

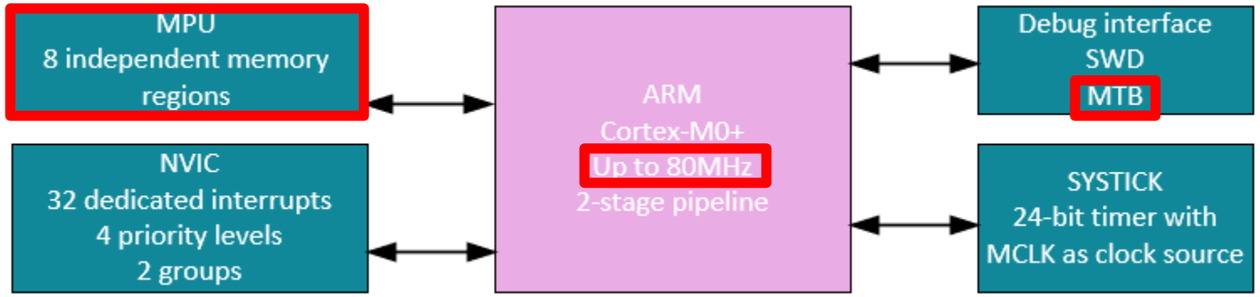


Fig2: MSPM0G CPU Block Diagram

MSPM0 CPU module in bus organization

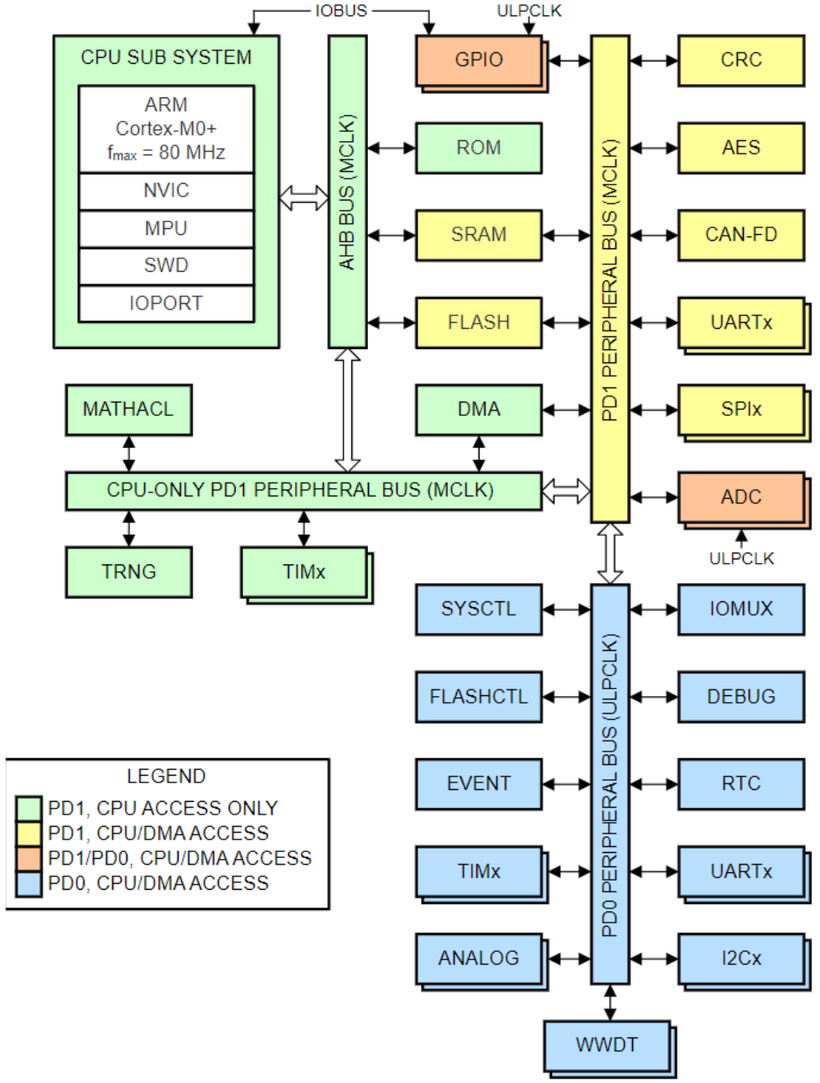


Fig1: MSPM0G Bus organization

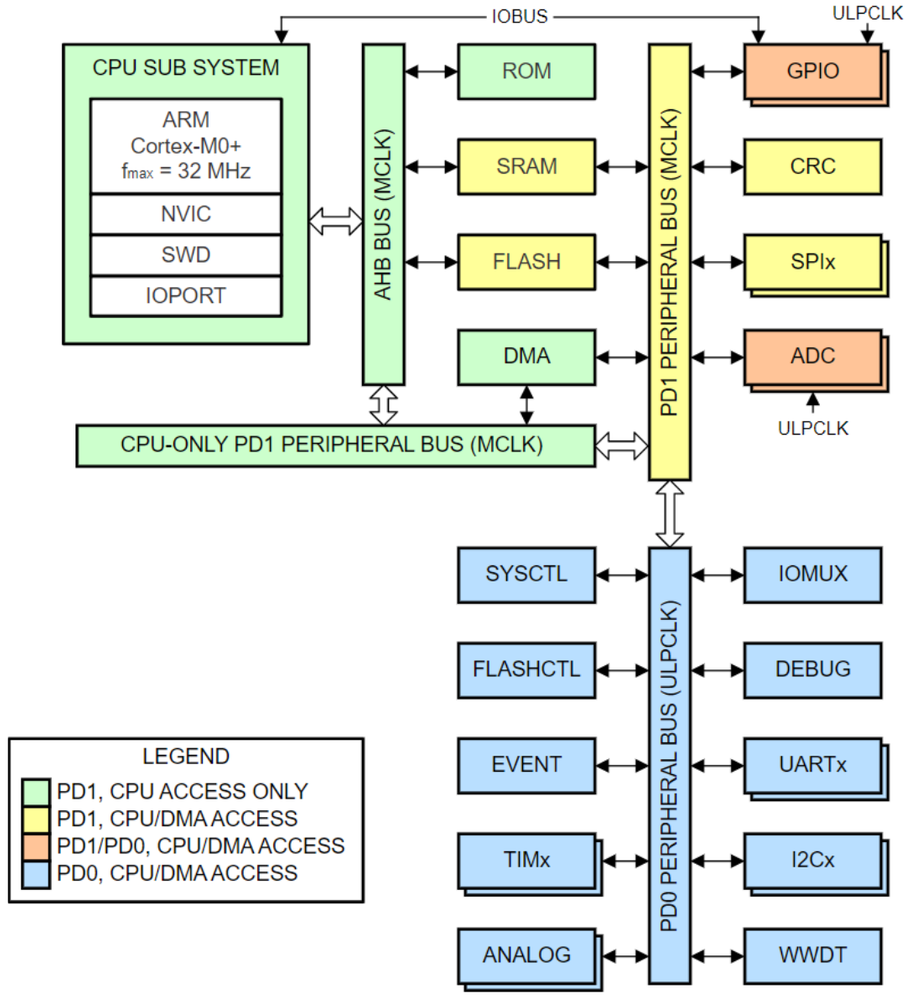


Fig2: MSPM0L Bus organization

To find more MSPM0 training series, please visit:

- TI.com.cn
- WeChat (德州仪器公众号)
- Bilibili
- 21IC