MSPM0 Low-power mode introduction
—— MSPM0 peripheral training series

Presented by Eason Zhou
### MCU Level Overview

**MSPM0Gxx Series**

**80 MHz MCU with up to 128kB flash, 64 pins, advanced analog, AES/TRNG, CAN-FD**

**Power Management and Clock Unit (PMCU)**
- System Controller (SYSCTL)
- Power Management (PMU)
- Clock Module (CKM)

**CPU**
- Arm Cortex-M0+
- 80 MHz

**Accelerators**
- Math (DIV, SQRT, TRIG, MAC)

**On-chip Memory**
- 32, 64, or 128 kB flash [ECC]
- 16 or 32 KB SRAM [ECC]

**Data Integrity & Security**
- CRC accelerator (16 and 32 bit)
- AES256 accelerator + TRNG

**Programming & Debug**
- ARM SWD interface
- UART & ICC bootloader

**Power & Clocking**
- POR / BOR / SVS
- External LF 32kHz XTAL
- External HF 44MHz XTAL
- Internal LF 32kHz (3%)
- Internal HF 432MHz (1%)
- PLL (up to 80 MHz)

**Communication**
- UART w/ LIN (1)
- UART (3)
- SPI (2)
- I2C (2) w/ FastMode+
- CAN-FD (1)

**Precision Analog**
- 12-bit ADC 4Mps (9-ch)
- 12-bit ADC 4Mps (8-ch)
- Compare w/ 2 8-bit DACs (3)
- 12-bit 1Msps buffered DAC (1)
- Zero-drift chopper op-amps (2)
- Internal reference (1.5%)
- General purpose amp (1)
- Temperature sensor

**Timers**
- Advanced control 16-bit 4 CC (1)
- Advanced control 16-bit 2 CC (1)
- General purpose 32-bit 2 CC (1)
- General purpose 16-bit 2 CC (2)
- Low power 16-bit 2 CC (2)
- Windowed watching (2)
- Real-time clock (1)

**Leaded packages:** VSOP-20/28, LOFP-48/64
**No-lead packages:** QFN-24/32/48, nFBGA-64, WQSP-28
MSPM0 PMCU overview

**PMCU Introduction**

**Power management and clock unit (PMCU):**
- Provides power, clocking, reset, and system control services for MPSM0
- Contains three submodules: SYSCTL, PMU, CKM

**System controller (SYSCTL):**
- PMU and CKM configuration
- Peripherals reset and enable
- CPU reset and enable
- Flash and SRAM control

**Power management (PMU):**
- Power supply to PD0 peripherals and PD1 peripherals
- Power supply to GPIO
- Power supply to analog peripherals
- Voltage reference
- Temperature sensor

**Clock module (CKM):**
- Clock supply
Low-power mode introduction

PD0 and PD1 Introduction

PD0 domain:
- Includes the PD0 peripherals (I2C / OPA / Timer) and PD0 peripheral bus

PD1 domain:
- Include the CPU sub system, SRAM, Flash, PD1 peripherals (SPI / DMA / ADC / Timer) and the PD1 peripheral bus

Power Mode Introduction

<table>
<thead>
<tr>
<th>Power Mode</th>
<th>Max Frequency</th>
<th>Base Idd</th>
<th>Functionality</th>
</tr>
</thead>
</table>
| RUN        | 24 / 32 / 80MHz | ≈85µA/MHz | • CPU is running  
|            |               |          | • All clocks and peripherals are available |
| SLEEP      | 24 / 32 / 80MHz | ≈200µA  | • Only CPU is disabled  
|            |               |          | • All clocks are available |
| STOP       | 4MHz | ≈50µA  | • PD0 peripherals are available  
|            |               |          | • PD1 peripherals are disabled with retention  
|            |               |          | • Available clocks: MFCLK (4MHz) or LFCLK (32KHz) |
| STANDBY    | 32KHz | ≈1µA  | • PD0 peripherals are available  
|            |               |          | • PD1 peripherals are disabled with retention  
|            |               |          | • Flash and SRAM is disabled with retention  
|            |               |          | • Available clock: LFCLK (32KHz) |
| SHUT DOWN  | No clocks | ≈50nA  | • All PD0 / PD1 peripherals are off  
|            |               |          | • Flash and SRAM are off  
|            |               |          | • Only NRST pin and wakeup IOs can wake MSPM0  
|            |               |          | • No available clock |

MSPM0

- CPU
- GPIO
- PD0 peripherals
- PD1 peripherals
- PMCU
- Power Control
- clock
- BOR wake
Power mode usage

• Run mode:

![Run mode diagram]

• Low-power mode (Standby):

![Low-power mode (Standby) diagram]
**MSPM0 Reset level introduction**

**POR and BOR Introduction**

**Power-on reset (POR):**
- Indicate VDD has reached sufficient voltage to start BOR circuit

**User-programmable brownout reset (BOR):**
- Ensures VDD is maintained at a sufficient voltage to support correct operation of the device
- Four selectable BOR threshold levels (BOR0-BOR3)

**Reset Level Introduction**

<table>
<thead>
<tr>
<th>Reset name</th>
<th>Trigger examples</th>
<th>Effect</th>
</tr>
</thead>
<tbody>
<tr>
<td>POR (Power-on reset)</td>
<td>• NRST (&gt; 1s) • VDD&lt;POR-</td>
<td>• Reset shutdown memory • Re-enable NRST/SWD pin function • Trigger BOR</td>
</tr>
<tr>
<td>BOR (brownout reset)</td>
<td>• VDD&lt;BOR- • SHUTDOWN exit</td>
<td>• Reset PMU • Reset all of the core logic • Trigger BOOTRST</td>
</tr>
<tr>
<td>BOOTRST (Boot reset)</td>
<td>• NRST (&lt; 1s) • Software</td>
<td>• Execute device boot configuration routine • Reset the majority of the core logic • Clear SRAM • Trigger SYSRST</td>
</tr>
<tr>
<td>SYSRST (System reset)</td>
<td>• WDT violation • Software • Debugger</td>
<td>• Reset CPU • Reset peripherals</td>
</tr>
<tr>
<td>CPURST (CPU reset)</td>
<td>• Software • Debugger</td>
<td>• Reset CPU</td>
</tr>
</tbody>
</table>

**POR and BOR Trigger Examples**

- **POR (Power-on reset):**
  - NRST (> 1s)
  - VDD<POR-
  - Trigger POR

- **BOR (Brownout Reset):**
  - VDD<BOR-
  - SHUTDOWN exit

- **BOOTRST (Boot Reset):**
  - NRST (< 1s)
  - Software

- **SYSRST (System Reset):**
  - WDT violation
  - Software
  - Debugger

- **CPURST (CPU Reset):**
  - Software
  - Debugger
PMCU module quick start

Academy
- Low-power mode introduction lab

Driverlib Examples
- MSPM0G350x:
  - `sysctl_power_policy_sleep_to_standby`
  - `sysctl_power_policy_sleep_to_stop`
  - `sysctl_shutdown`

- MSPM0L13xx:
  - `sysctl_power_policy_sleep_to_standby`
  - `sysctl_power_policy_sleep_to_stop`
  - `sysctl_shutdown`

Related Links
- MSPM0 online resource
- MSPM0 quick start guide
- MSPM0 Sysconfig user’s guide
- MSPM0G350x datasheet
- MSPM0L13xx datasheet
- MSPM0Gxx technical reference manual
- MSPM0Lxx technical reference manual

Launchpad
- LP-MSPM0G3507
- LP-MSPM0L1306

Sysconfig Entrance for PMCU Setting

Step 1:
- Select SYSTICK

Step 2:
- Power & Systems Configuration
- Power Policy: SLEEP0
- BOR Threshold: 0
- Enable Write Lock
- Enable Sleep On Exit
- Enable Event on Pending
- Disable NIRQ Pin
- FCC Configuration
- Flash Configuration (FlashCtl Configuration)
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